PENTIUM® PROCESSOR WITH MMX™ TECHNOLOGY

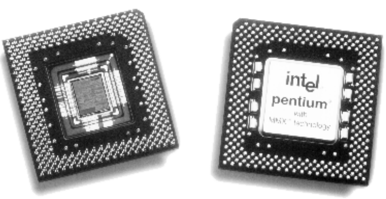
Maximum Operating Frequency	166 MHz	200 MHz	233 MHz
iCOMP® Index 2.0 Rating	160	182	203

NOTE: Contact Intel Corporation for more information about iCOMP® Index 2.0 ratings.

- **Support for MMX™ Technology**
- **Compatible with Large Software Base**
  - **MS-DOS*, Windows*, OS/2*, UNIX***
- **32-Bit Processor with 64-Bit Data Bus**
- **Superscalar Architecture**
  - **Enhanced Pipelines**
  - **Two Pipelined Integer Units Capable of Two Instructions per Clock**
  - **Pipelined MMX Unit**
  - **Pipelined Floating-Point Unit**
- **Separate Code and Data Caches**
  - **16-Kbyte Code, 16-Kbyte Write Back Data**
  - **MESI Cache Protocol**
- **Advanced Design Features**
  - **Deeper Write Buffers**
  - **Enhanced Branch Prediction Feature**
  - **Virtual Mode Extensions**
- **Enhanced CMOS Silicon Technology**
- **4-Mbyte Pages for Increased TLB Hit Rate**
- **IEEE 1149.1 Boundary Scan**
- **Dual Processing Configuration**
- **Internal Error Detection Features**
- **Multi-Processor Support**
  - **Multiprocessor Instructions**
  - **Support for Second Level Cache**
- **On-Chip Local APIC Controller**
  - **MP Interrupt Management**
  - **8259 Compatible**
- **Power Management Features**
  - **System Management Mode**
  - **Clock Control**
- **Fractional Bus Operation**
  - **233 MHz Core/66 MHz Bus**
  - **200 MHz Core/66 MHz Bus**
  - **166 MHz Core/66 MHz Bus**

The Pentium® processor with MMX™ technology extends the Pentium processor family, providing performance needed for mainstream desktop applications as well as for workstations. The Pentium processor with MMX technology is compatible with the entire installed base of applications for MS-DOS*, Windows*, OS/2* and UNIX*. The Pentium processor with MMX technology is the first microprocessor to support Intel MMX technology. Furthermore, the Pentium processor with MMX technology superscalar architecture can execute two instructions per clock cycle. Enhanced branch prediction and separate caches also increase performance. The pipelined floating-point unit delivers workstation level performance. Separate code and data caches reduce cache conflicts while remaining software transparent. The Pentium processor with MMX technology has 4.5 million transistors and is built on Intel's enhanced CMOS silicon technology.

The Pentium processor with MMX technology may contain design defects or errors known as errata that may cause the product to deviate from published specifications. Current characterized errata are available on request.



The Pentium® Processor with MMX™ technology may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

Contact your local Intel sales office or your distributor to obtain the latest specifications and before placing your product order.

Copies of documents which have an ordering number and are referenced in this document, or other Intel literature, may be obtained from:

Intel Corporation
P.O. Box 7641
Mt. Prospect, IL 60056-7641

or call 1-800-879-4683
or visit Intel's website at http\\:www.intel.com

CONTENTS

1.0. MICROPROCESSOR ARCHITECTURE OVERVIEW

The Pentium® processor with MMX™ technology extends the Intel Pentium family of microprocessors. It is binary compatible with the 8086/88, 80286, Intel386™ DX, Intel386 SX, Intel486™ DX, Intel486 SX, Intel486 DX2 and Pentium processors 60/66/75/90/100/120/133/150/166/200.

The Pentium processor family currently includes the following products.

- Pentium processor with MMX technology:
  - Pentium processor with MMX technology at 233 MHz, iCOMP® Index 2.0 rating = 203
  - Pentium processor with MMX technology at 200 MHz, iCOMP Index 2.0 rating = 182
  - Pentium processor with MMX technology at 166 MHz, iCOMP Index 2.0 rating = 160
- Pentium processor 133/150/166/200. The name "Pentium processor 133/150/166/200" will be used in this document to refer to the Pentium processor with 133, 150, 166 and 200 MHz versions of the Pentium processor:
  - Pentium processor at 200 MHz, iCOMP Index 2.0 rating = 142
  - Pentium processor at 166 MHz, iCOMP Index 2.0 rating = 127
  - Pentium processor at 150 MHz, iCOMP Index 2.0 rating = 114
  - Pentium processor at 133 MHz, iCOMP Index 2.0 rating = 111
  - Pentium processor at 120 MHz, iCOMP Index 2.0 rating = 100
  - Pentium processor at 100 MHz, iCOMP Index 2.0 rating = 90
  - Pentium processor at 90 MHz, iCOMP Index 2.0 rating = 81
  - Pentium processor at 75 MHz, iCOMP Index 2.0 rating = 67

The Pentium processor family supports the features of previous Intel Architecture processors, and provides significant enhancements and additions including the following:

- Superscalar Architecture
- Dynamic Branch Prediction
- Pipelined Floating-Point Unit
- Improved Instruction Execution Time
- Separate Code and Data Caches
- Writeback MESI Protocol in the Data Cache
- 64-Bit Data Bus
- Bus Cycle Pipelining
- Address Parity
- Internal Parity Checking
- Execution Tracing
- Performance Monitoring
- IEEE 1149.1 Boundary Scan
- System Management Mode
- Virtual Mode Extensions
- Dual processing support
- On-chip local APIC device

In addition to the features listed above, the Pentium processor with MMX technology offers the following enhancements over Pentium processor 133/150/166/200:

- Support for Intel MMX technology
- Doubled code and data cache sizes to 16 KB each
- Improved branch prediction
- Enhanced pipeline
- Deeper write buffers

The following features are supported by the Pentium processor 133/150/166/200, but these features are not supported by the Pentium processor with MMX technology:

- Functional redundancy check and Lock Step operation.
- Support for Intel 82498/82493 and 82497/82492 cache chipset products
- Split line accesses to the code cache

For a more detailed description of the Pentium processor family products, please refer to the *Pentium® Processor Family Developer's Manual* (Order Number 241428).

1.1. Pentium® Processor Family Architecture

The application instruction set of the Pentium processor family includes the complete Intel486 processor family instruction set with extensions to accommodate some of the additional functionality of the Pentium processors. All application software written for the Intel386 and Intel486 family microprocessors will run on the Pentium processors without modification. The on-chip memory management unit (MMU) is completely compatible with the Intel386 family and Intel486 family of processors.

The Pentium processors implement several enhancements to increase performance. The two instruction pipelines and floating-point unit on Pentium processors are capable of independent operation. Each pipeline issues frequently used instructions in a single clock. Together, the dual pipes can issue two integer instructions in one clock, or one floating-point instruction (under certain circumstances, two floating-point instructions) in one clock.

Branch prediction is implemented in the Pentium processors. To support this, Pentium processors implement two prefetch buffers, one to prefetch code in a linear fashion, and one that prefetches code according to the BTB so the needed code is almost always prefetched before it is needed for execution.

The floating-point unit has been completely redesigned over the Intel486 processor. Faster algorithms provide up to 10X speed-up for common operations including add, multiply and load.

Pentium processors include separate code and data caches are integrated on-chip to meet performance goals. Each cache has a 32-byte line size. Each cache has a dedicated Translation Lookaside Buffer (TLB) to translate linear addresses to physical addresses. The data cache is configurable to be write back or write through on a line-by-line basis and follows the MESI protocol. The data cache tags are triple ported to support two data transfers and an inquire cycle in the same clock. The code cache is an inherently write-protected cache. The code cache tags are multi-ported to support snooping. Individual pages can be configured as cacheable or non-cacheable by software or hardware. The caches can be enabled or disabled by software or hardware.

The Pentium processors have increased the data bus to 64 bits to improve the data transfer rate. Burst read and burst write back cycles are supported by the Pentium processors. In addition, bus cycle pipelining has been added to allow two bus cycles to be in progress simultaneously. The Pentium processors' Memory Management Unit contains optional extensions to the architecture which allow 4-Kbyte and 4-Mbyte page sizes.

The Pentium processors have added significant data integrity and error detection capability. Data parity checking is still supported on a byte-by-byte basis. Address parity checking and internal parity checking features have been added along with a new exception, the machine check exception.

As more and more functions are integrated on chip, the complexity of board level testing is increased. To address this, the Pentium processors have increased test and debug capability. The Pentium processors implement IEEE Boundary Scan (Standard 1149.1). In addition, the Pentium processors have specified 4 breakpoint pins that correspond to each of the debug registers and externally indicate a breakpoint match. Execution tracing provides external indications when an instruction has completed execution in either of the two internal pipelines, or when a branch has been taken.

System Management Mode (SMM) has been implemented along with some extensions to the SMM architecture. Enhancements to the virtual 8086 mode have been made to increase performance by reducing the number of times it is necessary to trap to a virtual 8086 monitor.

Figure 1 shows a block diagram of the Pentium processor with MMX technology as a representative of the Pentium processor family.

The block diagram shows the two instruction pipelines, the "u" pipe and the "v" pipe. The u-pipe can execute all integer and floating-point instructions. The v-pipe can execute simple integer instructions and the FXCH floating-point instructions.

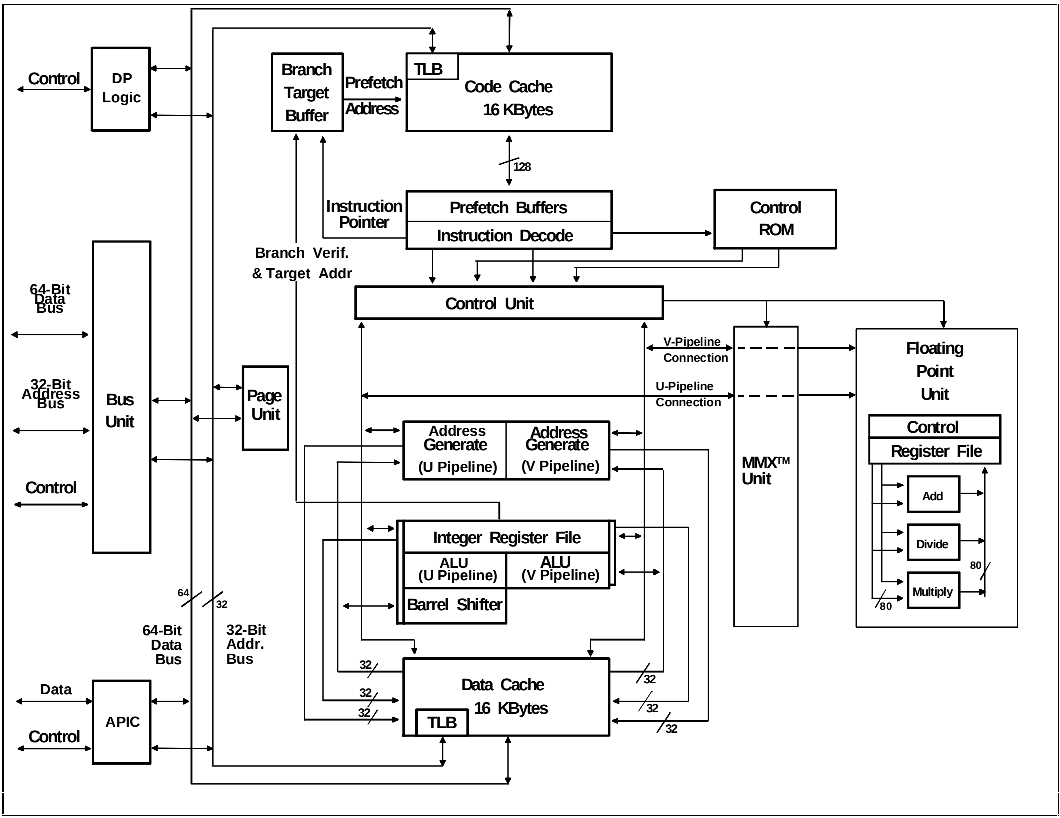


Figure 1. Pentium® Processor with MMX™ Technology Block Diagram

The separate code and data caches are shown. The data cache has two ports, one for each of the two pipes (the tags are triple ported to allow simultaneous inquire cycles). The data cache has a dedicated Translation Lookaside Buffer (TLB) to translate linear addresses to the physical addresses used by the data cache.

The code cache, branch target buffer and prefetch buffers are responsible for getting raw instructions into the execution units of the Pentium processor. Instructions are fetched from the code cache or from the external bus. Branch addresses are remembered by the branch target buffer. The code cache TLB translates linear addresses to physical addresses used by the code cache.

The decode unit decodes the prefetched instructions so the Pentium processors can execute the instruction. The control ROM contains the microcode which controls the sequence of operations that must be performed to implement the Pentium processor architecture. The control ROM unit has direct control over both pipelines.

The Pentium processors contain a pipelined floating-point unit that provides a significant floating-point performance advantage over previous generations of processors.

Symmetric dual processing in a system is supported with two Pentium processors. The two processors appear to the system as a single Pentium processor. Operating systems with dual processing support properly schedule computing tasks between the two processors. This scheduling of tasks is transparent to software applications and the end-user. Logic built into the processors support a "glueless" interface for

easy system design. Through a private bus, the two Pentium processors arbitrate for the external bus and maintain cache coherency. Dual processing is supported in a system only if both processors are operating at identical core and bus frequencies.

In this document, in order to distinguish between two Pentium processors in dual processing mode, one processor will be designated as the "Primary" processor and the other as the "Dual" processor.

The Pentium processors are produced on the enhanced 0.35 µm CMOS process which allows high device density and lower power dissipation. In addition to the SMM features described above, the Pentium processor supports clock control. When the clock to the Pentium processor is stopped, power dissipation is virtually eliminated. The combination of these improvements makes the Pentium processor a good choice for energy-efficient desktop designs.

The Pentium processor supports fractional bus operation. This allows the internal processor core to operate at high frequencies, while communicating with the external bus at lower frequencies.

The Pentium processor contains an on-chip Advanced Programmable Interrupt Controller (APIC). This APIC implementation supports multiprocessor interrupt management (with symmetric interrupt distribution across all processors), multiple I/O subsystem support, 8259A compatibility, and inter-processor interrupt support.

The architectural features introduced in this chapter are more fully described in the *Pentium® Processor Family Developer's Manual* (Order Number 241428).

1.2. Pentium® Processor with MMX™ Technology

The Pentium processor with MMX technology is a significant addition to the Pentium processor family. Available at 166, 200 and 233 MHz, it is the first microprocessor to support Intel's MMX technology.

The Pentium processor with MMX technology is both software and pin compatible with previous members of the Pentium processor family. It contains 4.5 million transistors and is manufactured on Intel's enhanced 0.35 micron CMOS process which allows voltage reduction technology for low power and high density. This enables the Pentium processor with MMX technology to remain within the thermal envelope of the original Pentium processor while providing a significant performance increase.

In addition to the architecture described in the previous section for the Pentium processor family, the Pentium processor with MMX technology has several additional micro-architectural enhancements, compared to the Pentium processor 133/150/166/200, which are described below:

1.2.1. FULL SUPPORT FOR INTEL MMX™ TECHNOLOGY

MMX technology is based on the Single Instruction Multiple Data (SIMD) technique which enables increased performance on a wide variety of multimedia and communications applications. Fifty-seven new instructions and four new 64-bit data types are supported in the Pentium processor with MMX technology. All existing operating system and application software are fully-compatible with the Pentium processor with MMX technology.

1.2.2. DOUBLE CODE AND DATA CACHES TO 16K EACH

On-chip level-1 data and code cache sizes have been doubled to 16 KB each and are 4-way set associative on the Pentium processor with MMX technology. Larger separate internal caches improve performance by reducing average memory access time and providing fast access to recently-used instructions and data. The instruction and data caches can be accessed simultaneously while the data cache supports two data references simultaneously. The data cache supports a write-back (or alternatively, write-through, on a line by line basis) policy for memory updates.

1.2.3. IMPROVED BRANCH PREDICTION

Dynamic branch prediction uses the Branch Target Buffer (BTB) to boost performance by predicting the most likely set of instructions to be executed. The BTB has been improved on the Pentium processor with MMX technology to increase its accuracy. Further, the Pentium processor with MMX technology has four prefetch buffers that can hold up to four successive code streams.

1.2.4. ENHANCED PIPELINE

An additional pipeline stage has been added and the pipeline has been enhanced to improve performance.

The integration of the MMX pipeline with the integer pipeline is very similar to that of the floating-point pipeline. Under some circumstances, two MMX instructions or one integer and one MMX instruction can be paired and issued in one clock cycle to increase throughput.

The enhanced pipeline is described in more detail in the *Pentium® Processor Family Developer's Manual* (Order Number 241428).

1.2.5. DEEPER WRITE BUFFERS

A pool of four write buffers is now shared between the dual pipelines to improve memory write performance.

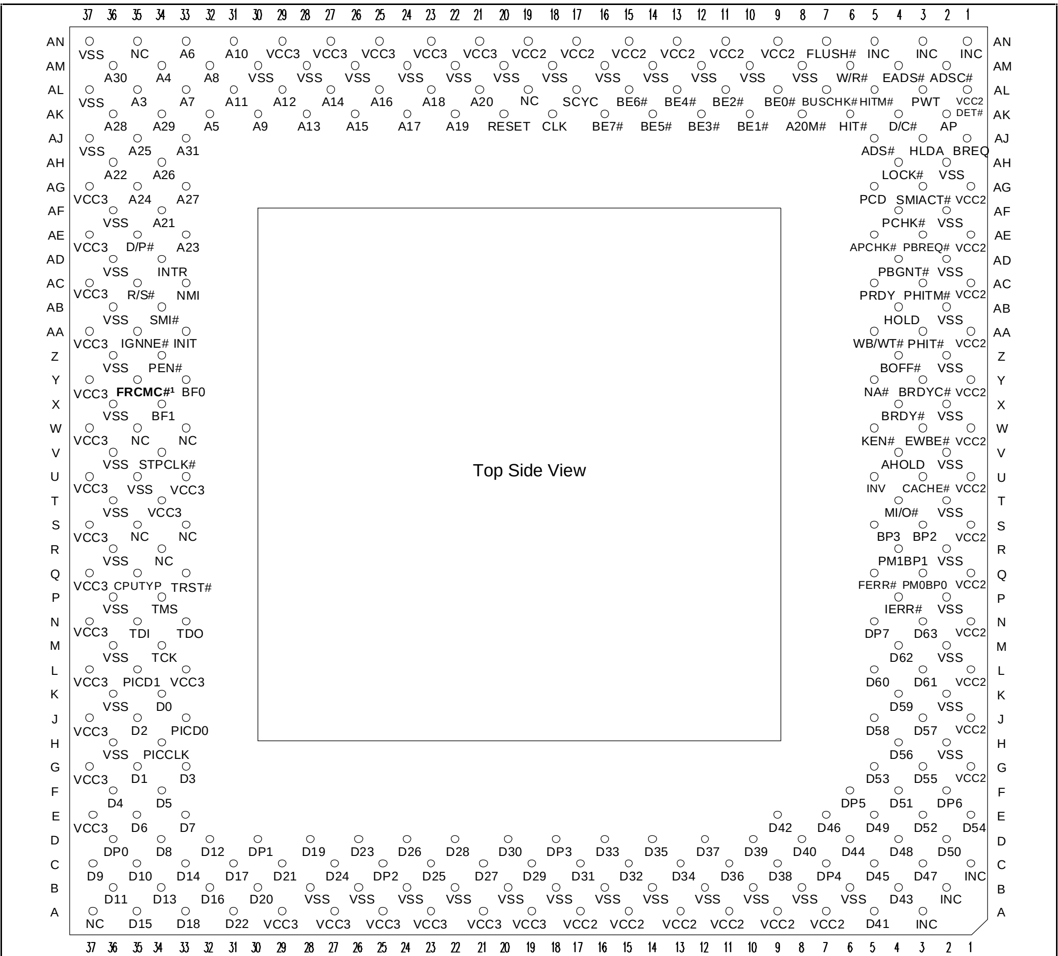
1.3. Mobile Pentium® Processor with MMX™ Technology

Currently, Intel's Mobile Pentium processor with MMX technology family consists of three products. Detailed information on Mobile Pentium processors with MMX technology based on the enhanced CMOS process technology is available in the datasheet *Mobile Pentium® Processor with MMX™ Technology* (Order Number 243292). Please reference the datasheet for correct pinout, mechanical, thermal and electrical specifications.

2.0. PINOUT

2.1. Pinout and Pin Descriptions

2.1.1. PENTIUM® PROCESSOR WITH MMX™ TECHNOLOGY PINOUT

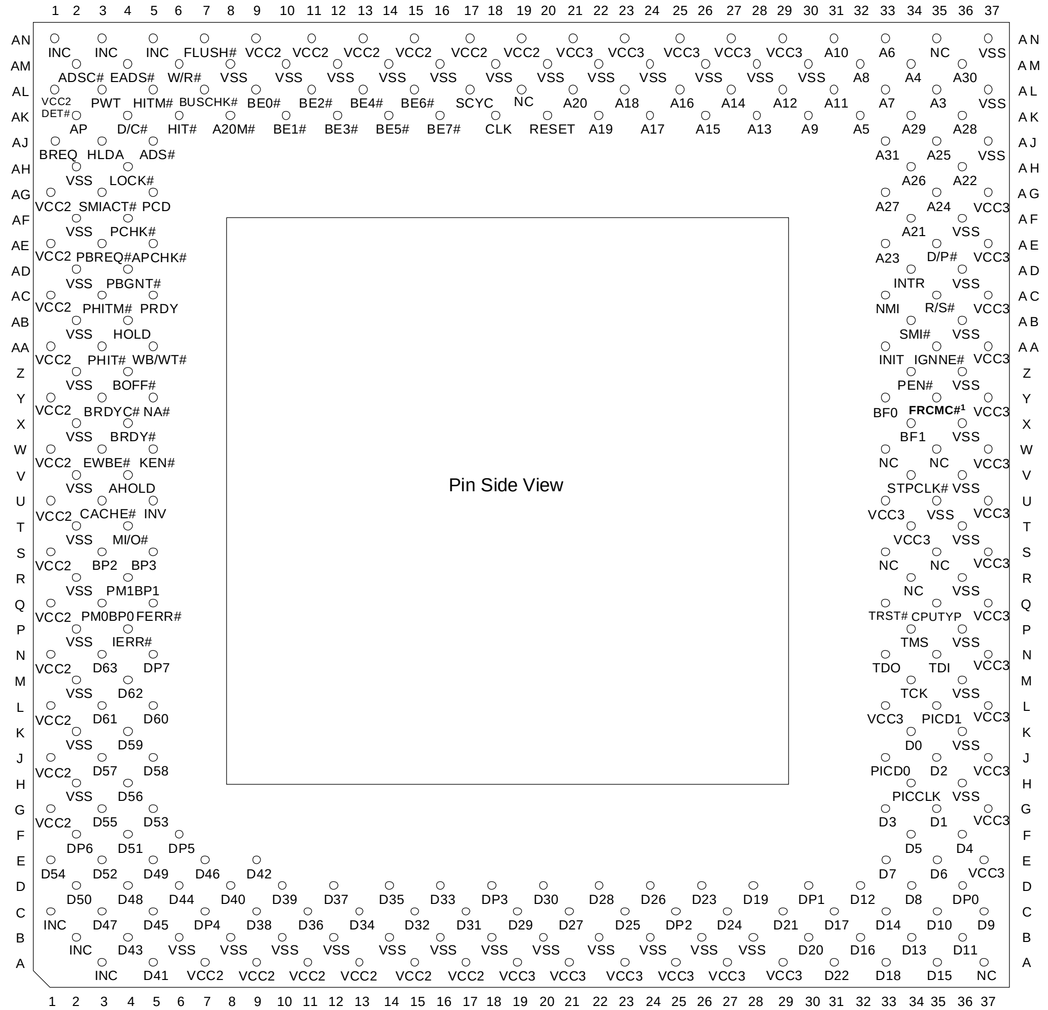


NOTE:

1. The FRCMC# pin is not defined for Pentium® processor with MMX™ technology. Pin Y35 should be left as a "NC" or tied to V_{CC3} via an external pull-up resistor.

PP0008a

Figure 2. Pentium® Processor with MMX™ Technology SPGA and PPGA Package Pinout (Top Side View)



NOTE:

1. The FRCMC# pin is not defined for Pentium® processor with MMX™ technology. Pin Y35 should be left as a "NC" or tied to V_{CC3} via an external pull-up resistor.

Figure 3. Pentium® Processor with MMX™ Technology SPGA and PPGA Package Pinout (Pin Side View)

2.1.2. PIN CROSS-REFERENCE TABLE FOR PENTIUM® PROCESSOR WITH MMX™

Table 1. Pin Cross-Reference by Pin Name (xPGA Package)

Address									
A3	AL35	A9	AK30	A15	AK26	A21	AF34	A27	AG33
A4	AM34	A10	AN31	A16	AL25	A22	AH36	A28	AK36
A5	AK32	A11	AL31	A17	AK24	A23	AE33	A29	AK34
A6	AN33	A12	AL29	A18	AL23	A24	AG35	A30	AM36
A7	AL33	A13	AK28	A19	AK22	A25	AJ35	A31	AJ33
A8	AM32	A14	AL27	A20	AL21	A26	AH34		

Data									
D0	K34	D13	B34	D26	D24	D39	D10	D52	E03
D1	G35	D14	C33	D27	C21	D40	D08	D53	G05
D2	J35	D15	A35	D28	D22	D41	A05	D54	E01
D3	G33	D16	B32	D29	C19	D42	E09	D55	G03
D4	F36	D17	C31	D30	D20	D43	B04	D56	H04
D5	F34	D18	A33	D31	C17	D44	D06	D57	J03
D6	E35	D19	D28	D32	C15	D45	C05	D58	J05
D7	E33	D20	B30	D33	D16	D46	E07	D59	K04
D8	D34	D21	C29	D34	C13	D47	C03	D60	L05
D9	C37	D22	A31	D35	D14	D48	D04	D61	L03
D10	C35	D23	D26	D36	C11	D49	E05	D62	M04
D11	B36	D24	C27	D37	D12	D50	D02	D63	N03
D12	D32	D25	C23	D38	C09	D51	F04		

Table 1. Pin Cross-Reference by Pin Name (xPGA Package)(Cont'd)

Control							
A20M#	AK08	BREQ	AJ01	HIT#	AK06	PRDY	AC05
ADS#	AJ05	BUSCHK#	AL07	HITM#	AL05	PWT	AL03
ADSC#	AM02	CACHE#	U03	HLDA	AJ03	R/S#	AC35
AHOLD	V04	CPUTYP	Q35	HOLD	AB04	RESET	AK20
AP	AK02	D/C#	AK04	IERR#	P04	SCYC	AL17
APCHK#	AE05	D/P#	AE35	IGNNE#	AA35	SMI#	AB34
BE0#	AL09	DP0	D36	INIT	AA33	SMIACT#	AG03
BE1#	AK10	DP1	D30	INTR/LINT0	AD34	TCK	M34
BE2#	AL11	DP2	C25	INV	U05	TDI	N35
BE3#	AK12	DP3	D18	KEN#	W05	TDO	N33
BE4#	AL13	DP4	C07	LOCK#	AH04	TMS	P34
BE5#	AK14	DP5	F06	M/IO#	T04	TRST#	Q33
BE6#	AL15	DP6	F02	NA#	Y05	VCC2DET#	AL01
BE7#	AK16	DP7	N05	NMI/LINT1	AC33	W/R#	AM06
BOFF#	Z04	EADS#	AM04	PCD	AG05	WB/WT#	AA05
BP2	S03	EWBE#	W03	PCHK#	AF04		
BP3	S05	FERR#	Q05	PEN#	Z34		
BRDY#	X04	FLUSH#	AN07	PM0/BP0	Q03		
BRDYC#	Y03	FRCMC#[1]	Y35	PM1/BP1	R04		

APIC		Clock Control		Dual Processor Private Interface			
PICCLK	H34 (2)	CLK	AK18 (2)	PBGNT#	AD04		
PICD0	J33	[BF0]	Y33	PBREQ#	AE03		
[DPEN#]		[BF1]	X34	PHIT#	AA03		
PICD1	L35	STPCLK#	V34	PHITM#	AC03		
[APICEN]							

V_{CC2}				
A17	A07	Q01	AA01	AN11
A15	G01	S01	AC01	AN13
A13	J01	U01	AE01	AN15
A11	L01	W01	AG01	AN17
A09	N01	Y01	AN09	AN19

Table 1. Pin Cross-Reference by Pin Name (xPGA Package)(Cont'd)

V_{CC3}						
A19	A27	J37	Q37	U37	AC37	AN27
A21	A29	L37	S37	W37	AE37	AN25
A23	E37	L33	T34	Y37	AG37	AN23
A25	G37	N37	U33	AA37	AN29	AN21

V_{SS}								
B06	B18	H02	P02	U35	Z36	AF36	AM12	AM24
B08	B20	H36	P36	V02	AB02	AH02	AM14	AM26
B10	B22	K02	R02	V36	AB36	AJ37	AM16	AM28
B12	B24	K36	R36	X02	AD02	AL37	AM18	AM30
B14	B26	M02	T02	X36	AD36	AM08	AM20	AN37
B16	B28	M36	T36	Z02	AF02	AM10	AM22	

NC		
A37	S35	AL19
R34	W33	AN35
S33	W35	—

INC					
A03	B02	C01	AN01	AN03	AN05

NOTES:

1. The FRCMC# pin is not defined for the Pentium® processor with MMX™ technology. This pin should be left as a "NC" or tied to V_{CC3} via an external pull-up resistor on the Pentium processor with MMX technology.
2. PICCLK and CLK are 3.3V-tolerant-only on the Pentium processor with MMX technology. Please refer to the *Pentium® Processor Family Developer's Manual* (Order Number 241428) for the CLK and PICCLK signal quality specification.

2.2. Design Notes

For reliable operation, always connect unused inputs to an appropriate signal level. Unused active low inputs should be connected to V_{CC3}. Unused active high inputs should be connected to GND.

No Connect (NC) pins must remain unconnected. Connection of NC or INC pins may result in component failure or incompatibility with processor steppings.

2.3. Quick Pin Reference

This section gives a brief functional description of each of the pins. For a detailed description, see the Hardware Interface chapter in the *Pentium® Processor Family Developer's Manual* (Order Number 241428).

NOTE

All input pins must meet their AC/DC specifications to guarantee proper functional behavior.

The # symbol at the end of a signal name indicates that the active, or asserted state occurs when the signal is at a low voltage. When a # symbol is not present after the signal name, the signal is active, or asserted at the high voltage level. Square brackets around a signal name indicate that the signal is defined only at RESET.

The following pins become I/O pins when two Pentium processors with MMX technology are operating in a dual processing environment:

ADS#, CACHE#, HIT#, HITM#, HLDA#, LOCK#, M/IO#, D/C#, W/R#, SCYC, BE#4

Table 2. Quick Pin Reference

Symbol	Type	Name and Function
A20M#	I	When the **address bit 20 mask** pin is asserted, the Pentium® processor with MMX™ technology emulates the address wraparound at 1 Mbyte which occurs on the 8086 by masking physical address bit 20 (A20) before performing a lookup to the internal caches or driving a memory cycle on the bus. The effect of A20M# is undefined in protected mode. A20M# must be asserted only when the processor is in real mode. A20M# is internally masked by the Pentium processor with MMX technology when configured as a Dual processor.
A31-A3	I/O	As outputs, the **address** lines of the processor along with the byte enables define the physical area of memory or I/O accessed. The external system drives the inquire address to the processor on A31-A5.
ADS#	O	The **address strobe** indicates that a new valid bus cycle is currently being driven by the Pentium processor with MMX technology.
ADSC#	O	The **address strobe (copy)** is functionally identical to ADS#.
AHOLD	I	In response to the assertion of **address hold**, the Pentium processor with MMX technology will stop driving the address lines (A31-A3) and AP in the next clock. The rest of the bus will remain active so data can be returned or driven for previously issued bus cycles.
AP	I/O	**Address parity** is driven by the Pentium processor with MMX technology with even parity information on all Pentium processor with MMX technology generated cycles in the same clock that the address is driven. Even parity must be driven back to the Pentium processor with MMX technology during inquire cycles on this pin in the same clock as EADS# to ensure that correct parity check status is indicated by the Pentium processor with MMX technology.
APCHK#	O	The **address parity check** status pin is asserted two clocks after EADS# is sampled active if the Pentium processor with MMX technology has detected a parity error on the address bus during inquire cycles. APCHK# will remain active for one clock each time a parity error is detected (including during dual processing private snooping).
[APICEN] PICD1	I	**Advanced Programmable Interrupt Controller Enable** enables or disables the on-chip APIC interrupt controller. If sampled high at the falling edge of RESET, the APIC is enabled. APICEN shares a pin with the PICD1 signal.

Table 2. Quick Pin Reference (Cont'd)

Symbol	Type	Name and Function
BE7#–BE4# BE3#–BE0#	O I/O	The **byte enable** pins are used to determine which bytes must be written to external memory or which bytes were requested by the CPU for the current cycle. The byte enables are driven in the same clock as the address lines (A31-3). Additionally, the lower 4-byte enables (BE3#-BE0#) are used on the Pentium processor with MMX technology as APIC ID inputs and are sampled at RESET. In dual processing mode, BE4# is used as an input during Flush cycles.
BF[1:0]	I	The **bus frequency** pins determine the bus-to-core frequency ratio. BF[1:0] are sampled at RESET, and cannot be changed until another non-warm (1 ms) assertion of RESET. Additionally, BF[1:0] must not change values while RESET is active. See Table 3 for Bus Frequency Selections.
BOFF#	I	The **backoff** input is used to abort all outstanding bus cycles that have not yet completed. In response to BOFF#, the Pentium processor with MMX technology will float all pins normally floated during bus hold in the next clock. The processor remains in bus hold until BOFF# is negated, at which time the Pentium processor with MMX technology restarts the aborted bus cycle(s) in their entirety.
BP[3:2] PM/BP[1:0]	O	The **breakpoint** pins (BP3-0) correspond to the debug registers, DR3-DR0. These pins externally indicate a breakpoint match when the debug registers are programmed to test for breakpoint matches. BP1 and BP0 are multiplexed with the **performance monitoring** pins (PM1 and PM0). The PB1 and PB0 bits in the Debug Mode Control Register determine if the pins are configured as breakpoint or performance monitoring pins. The pins come out of RESET configured for performance monitoring.
BRDY#	I	The **burst ready** input indicates that the external system has presented valid data on the data pins in response to a read or that the external system has accepted the Pentium processor with MMX technology data in response to a write request. This signal is sampled in the T2, T12 and T2P bus states.
BRDYC#	I	The **burst ready (copy)** is functionally identical to BRDY#.
BREQ	O	The **bus request** output indicates to the external system that the Pentium processor with MMX technology has internally generated a bus request. This signal is always driven whether or not the Pentium processor with MMX technology is driving its bus.

Table 2. Quick Pin Reference (Cont'd)

Symbol	Type	Name and Function
BUSCHK#	I	The **bus check** input allows the system to signal an unsuccessful completion of a bus cycle. If this pin is sampled active, the Pentium processor with MMX technology will latch the address and control signals in the machine check registers. If, in addition, the MCE bit in CR4 is set, the Pentium processor with MMX technology will vector to the machine check exception. **NOTE:** To assure that BUSCHK# will always be recognized, STPCLK# must be deasserted any time BUSCHK# is asserted by the system, before the system allows another external bus cycle. If BUSCHK# is asserted by the system for a snoop cycle while STPCLK# remains asserted, usually (if MCE=1) the processor will vector to the exception after STPCLK# is deasserted. But if another snoop to the same line occurs during STPCLK# assertion, the processor can lose the BUSCHK# request.
CACHE#	O	For Pentium processor with MMX technology-initiated cycles the **cache** pin indicates internal cacheability of the cycle (if a read), and indicates a burst write back cycle (if a write). If this pin is driven inactive during a read cycle, the Pentium processor with MMX technology will not cache the returned data, regardless of the state of the KEN# pin. This pin is also used to determine the cycle length (number of transfers in the cycle).
CLK	I	The **clock** input provides the fundamental timing for the Pentium processor with MMX technology. Its frequency is the operating frequency of the Pentium processor with MMX technology external bus, and requires TTL levels. All external timing parameters except TDI, TDO, TMS, TRST#, and PICD0-1 are specified with respect to the rising edge of CLK. This pin is 3.3V-tolerant-only on the Pentium processor with MMX technology. Please refer to the *Pentium® Processor Family Developer's Manual* (Order Number 241428) for the CLK and PICCLK signal quality specification. **NOTE:** It is recommended that CLK begin toggling within 150 ms after V_{CC} reaches its proper operating level. This recommendation is to ensure long-term reliability of the device.
CPUTYP	I	**CPU type** distinguishes the Primary processor from the Dual processor. In a single processor environment, or when the Pentium processor with MMX technology is acting as the Primary processor in a dual processing system, CPUTYP should be strapped to V_{SS}. The Dual processor should have CPUTYP strapped to V_{CC3}.
D/C#	O	The **data/code** output is one of the primary bus cycle definition pins. It is driven valid in the same clock as the ADS# signal is asserted. D/C# distinguishes between data and code or special cycles.

Table 2. Quick Pin Reference (Cont'd)

Symbol	Type	Name and Function
D/P#	O	The **dual/primary** processor indication. The Primary processor drives this pin low when it is driving the bus, otherwise it drives this pin high. D/P# is always driven. D/P# can be sampled for the current cycle with ADS# (like a status pin). This pin is defined only on the Primary processor. Dual processing is supported in a system only if both processors are operating at identical core and bus frequencies. Within these restrictions, two processors of different steppings may operate together in a system.
D63-D0	I/O	These are the 64 **data lines** for the processor. Lines D7-D0 define the least significant byte of the data bus; lines D63-D56 define the most significant byte of the data bus. When the CPU is driving the data lines, they are driven during the T2, T12, or T2P clocks for that cycle. During reads, the CPU samples the data bus when BRDY# is returned.
DP7-DP0	I/O	These are the **data parity** pins for the processor. There is one for each byte of the data bus. They are driven by the Pentium processor with MMX technology with even parity information on writes in the same clock as write data. Even parity information must be driven back to the Pentium processor with MMX technology on these pins in the same clock as the data to ensure that the correct parity check status is indicated by the Pentium processor with MMX technology. DP7 applies to D63-56, DP0 applies to D7-0.
[DPEN#] PICD0	I/O	**Dual processing enable** is an output of the Dual processor and an input of the Primary processor. The Dual processor drives DPEN# low to the Primary processor at RESET to indicate that the Primary processor should enable dual processor mode. DPEN# may be sampled by the system at the falling edge of RESET to determine if the dual-processor socket is occupied. DPEN# is multiplexed with PICD0.
EADS#	I	This signal indicates that a valid **external address** has been driven onto the Pentium processor with MMX technology address pins to be used for an inquire cycle.
EWBE#	I	The **external write buffer empty** input, when inactive (high), indicates that a write cycle is pending in the external system. When the Pentium processor with MMX technology generates a write, and EWBE# is sampled inactive, the Pentium processor with MMX technology will hold off all subsequent writes to all E- or M-state lines in the data cache until all write cycles have completed, as indicated by EWBE# being active.
FERR#	O	The **floating-point error** pin is driven active when an unmasked **floating-point** error occurs. FERR# is similar to the ERROR# pin on the Intel387™ math coprocessor. FERR# is included for compatibility with systems using DOS type **floating-point** error reporting. FERR# is never driven active by the Dual processor.

Table 2. Quick Pin Reference (Cont'd)

Symbol	Type	Name and Function
FLUSH#	I	When asserted, the **cache flush** input forces the Pentium processor with MMX technology to write back all modified lines in the data cache and invalidate its internal caches. A Flush Acknowledge special cycle will be generated by the Pentium processor with MMX technology indicating completion of the write back and invalidation. If FLUSH# is sampled low when RESET transitions from high to low, tristate test mode is entered. If two Pentium processors with MMX technology are operating in dual processing mode and FLUSH# is asserted, the Dual processor will perform a flush first (without a flush acknowledge cycle), then the Primary processor will perform a flush followed by a flush acknowledge cycle. **NOTE:** If the FLUSH# signal is asserted in dual processing mode, it must be deasserted at least one clock prior to BRDY# of the FLUSH Acknowledge cycle to avoid DP arbitration problems.
FRCMC#	I	Functional Redundancy Checking is not supported on thePentium processor with MMX technology. The FRCMC# pin is not defined for the Pentium processor with MMX technology. This pin should be left as a"NC" or tied to V_{CC3} via an external pull-up resistor.
HIT#	O	The **hit** indication is driven to reflect the outcome of an inquire cycle. If an inquire cycle hits a valid line in either the Pentium processor with MMX technology data or instruction cache, this pin is asserted two clocks after EADS# is sampled asserted. If the inquire cycle misses the Pentium processor with MMX technology cache, this pin is negated two clocks after EADS#. This pin changes its value only as a result of an inquire cycle and retains its value between the cycles.
HITM#	O	The **hit to a modified line** output is driven to reflect the outcome of an inquire cycle. It is asserted after inquire cycles which resulted in a hit to a modified line in the data cache. It is used to inhibit another bus master from accessing the data until the line is completely written back.
HLDA	O	The **bus hold acknowledge** pin goes active in response to a hold request driven to the processor on the HOLD pin. It indicates that the Pentium processor with MMX technology has floated most of the output pins and relinquished the bus to another local bus master. When leaving bus hold, HLDA will be driven inactive and the Pentium processor with MMX technology will resume driving the bus. If the Pentium processor with MMX technology has a bus cycle pending, it will be driven one clock cycle after HLDA is de-asserted.
HOLD	I	In response to the **bus hold request**, the Pentium processor with MMX technology will float most of its output and input/output pins and assert HLDA after completing all outstanding bus cycles. The Pentium processor with MMX technology will maintain its bus in this state until HOLD is de-asserted. HOLD is not recognized during LOCK cycles. The Pentium processor with MMX technology will recognize HOLD during reset.

Table 2. Quick Pin Reference (Cont'd)

Symbol	Type	Name and Function
IERR#	O	The **internal error** pin is used to indicate internal parity errors. If a parity error occurs on a read from an internal array, the Pentium processor with MMX technology will assert the IERR# pin for one clock and then shutdown.
IGNNE#	I	This is the **ignore numeric error** input. This pin has no effect when the NE bit in CR0 is set to 1. When the CR0.NE bit is 0, and the IGNNE# pin is asserted, the Pentium processor with MMX technology will ignore any pending unmasked numeric exception and continue executing floating-point instructions for the entire duration that this pin is asserted. When the CR0.NE bit is 0, IGNNE# is not asserted, a pending unmasked numeric exception exists (SW.ES = 1), and the floating-point instruction is one of FINIT, FCLEX, FSTENV, FSAVE, FSTSW, FSTCW, FENI, FDISI, or FSETPM, the Pentium processor with MMX technology will execute the instruction in spite of the pending exception. When the CR0.NE bit is 0, IGNNE# is not asserted, a pending unmasked numeric exception exists (SW.ES = 1), and the floating-point instruction is one other than FINIT, FCLEX, FSTENV, FSAVE, FSTSW, FSTCW, FENI, FDISI, or FSETPM, the Pentium processor with MMX technology will stop execution and wait for an external interrupt. IGNNE# is internally masked when the Pentium processor with MMX technology is configured as a Dual processor.
INIT	I	The Pentium processor with MMX technology **initialization** input pin forces the Pentium processor with MMX technology to begin execution in a known state. The processor state after INIT is the same as the state after RESET except that the internal caches, write buffers, and floating-point registers retain the values they had prior to INIT. INIT may NOT be used in lieu of RESET after power-up. If INIT is sampled high when RESET transitions from high to low, the Pentium processor with MMX technology will perform built-in self test prior to the start of program execution.
INTR/LINT0	I	An active **maskable interrupt** input indicates that an external interrupt has been generated. If the IF bit in the EFLAGS register is set, the Pentium processor with MMX technology will generate two locked interrupt acknowledge bus cycles and vector to an interrupt handler after the current instruction execution is completed. INTR must remain active until the first interrupt acknowledge cycle is generated to assure that the interrupt is recognized. If the local APIC is enabled, this pin becomes LINT0.
INV	I	The **invalidation** input determines the final cache line state (S or I) in case of an inquire cycle hit. It is sampled together with the address for the inquire cycle in the clock EADS# is sampled active.
KEN#	I	The **cache enable** pin is used to determine whether the current cycle is cacheable or not and is consequently used to determine cycle length. When the Pentium processor with MMX technology generates a cycle that can be cached (CACHE# asserted) and KEN# is active, the cycle will be transformed into a burst line fill cycle.

Table 2. Quick Pin Reference (Cont'd)

Symbol	Type	Name and Function
LINT0/INTR	I	If the APIC is enabled, this pin is **local interrupt 0**. If the APIC is disabled, this pin is INTR.
LINT1/NMI	I	If the APIC is enabled, this pin is **local interrupt 1**. If the APIC is disabled, this pin is NMI.
LOCK#	O	The **bus lock** pin indicates that the current bus cycle is locked. The Pentium processor with MMX technology will not allow a bus hold when LOCK# is asserted (but AHOLD and BOFF# are allowed). LOCK# goes active in the first clock of the first locked bus cycle and goes inactive after the BRDY# is returned for the last locked bus cycle. LOCK# is guaranteed to be de-asserted for at least one clock between back-to-back locked cycles.
M/IO#	O	The **memory/input-output** is one of the primary bus cycle definition pins. It is driven valid in the same clock as the ADS# signal is asserted. M/IO# distinguishes between memory and I/O cycles.
NA#	I	An active **next address** input indicates that the external memory system is ready to accept a new bus cycle although all data transfers for the current cycle have not yet completed. The Pentium processor with MMX technology will issue ADS# for a pending cycle two clocks after NA# is asserted. The Pentium processor with MMX technology supports up to 2 outstanding bus cycles.
NMI/LINT1	I	The **non-maskable interrupt** request signal indicates that an external non-maskable interrupt has been generated. If the local APIC is enabled, this pin becomes LINT1.
PBGNT#	I/O	**Private bus grant** is the grant line that is used when two Pentium processors with MMX technology are configured in dual processing mode, in order to perform private bus arbitration. PBGNT# should be left unconnected if only one Pentium processor with MMX technology exists in a system.
PBREQ#	I/O	**Private bus request** is the request line that is used when two Pentium processor with MMX technology are configured in dual processing mode, in order to perform private bus arbitration. PBREQ# should be left unconnected if only one Pentium processor with MMX technology exists in a system.
PCD	O	The **page cache disable** pin reflects the state of the PCD bit in CR3, the Page Directory Entry, or the Page Table Entry. The purpose of PCD is to provide an external cacheability indication on a page by page basis.
PCHK#	O	The **parity check** output indicates the result of a parity check on a data read. It is driven with parity status two clocks after BRDY# is returned. PCHK# remains low one clock for each clock in which a parity error was detected. Parity is checked only for the bytes on which valid data is returned. When two Pentium processors with MMX technology are operating in dual processing mode, PCHK# may be driven two or three clocks after BRDY# is returned.

Table 2. Quick Pin Reference (Cont'd)

Symbol	Type	Name and Function
PEN#	I	The **parity enable** input (along with CR4.MCE) determines whether a machine check exception will be taken as a result of a data parity error on a read cycle. If this pin is sampled active in the clock a data parity error is detected, the Pentium processor with MMX technology will latch the address and control signals of the cycle with the parity error in the machine check registers. If, in addition, the machine check enable bit in CR4 is set to"1", the Pentium processor with MMX technology will vector to the machine check exception before the beginning of the next instruction.
PHIT#	I/O	**Private hit** is a hit indication used when two Pentium processors with MMX technology are configured in dual processing mode, in order to maintain local cache coherency. PHIT# should be left unconnected if only one Pentium processor with MMX technology exists in a system.
PHITM#	I/O	**Private modified hit** is a hit on a modified cache line indication used when two Pentium processors with MMX technology are configured in dual processing mode, in order to maintain local cache coherency. PHITM# should be left unconnected if only one Pentium processor with MMX technology exists in a system.
PICCLK	I	The APIC interrupt controller serial data bus clock is driven into the **programmable interrupt controller clock** input of the Pentium processor with MMX technology. This pin is 3.3V-tolerant-only on the Pentium processor with MMX technology. Please refer to the *Pentium® Processor Family Developer's Manual* (Order Number 241428) for the CLK and PICCLK signal quality specification.
PICD0-1 [DPEN#] [APICEN]	I/O	**Programmable interrupt controller data lines 0-1** of the Pentium processor with MMX technology comprise the data portion of the APIC 3-wire bus. They are open-drain outputs that require external pull-up resistors. These signals are multiplexed with DPEN# and APICEN respectively.
PM/BP[1:0]	O	These pins function as part of the performance monitoring feature. The breakpoint 1-0 pins are multiplexed with the **performance monitoring 1-0** pins. The PB1 and PB0 bits in the Debug Mode Control Register determine if the pins are configured as breakpoint or performance monitoring pins. The pins come out of RESET configured for performance monitoring.
PRDY	O	The **probe ready** output pin is provided for use with the Intel debug port. Please refer to the *Pentium® Processor Family Developer's Manual* (Order Number 241428) for more details.
PWT	O	The **page write through** pin reflects the state of the PWT bit in CR3, the page directory entry, or the page table entry. The PWT pin is used to provide an external write back indication on a page-by-page basis.
R/S#	I	The **run/stop** input is provided for use with the Intel debug port. Please refer to the *Pentium® Processor Family Developer's Manual* (Order Number 241428) for more details.

Table 2. Quick Pin Reference (Cont'd)

Symbol	Type	Name and Function
RESET	I	**RESET** forces the Pentium processor with MMX technology to begin execution at a known state. All the Pentium processor with MMX technology internal caches will be invalidated upon the RESET. Modified lines in the data cache are not written back. FLUSH# and INIT are sampled when RESET transitions from high to low to determine if tristate test mode or checker mode will be entered, or if Built-In Self-Test (BIST) will be run.
SCYC	O	The **split cycle** output is asserted during misaligned LOCKed transfers to indicate that more than two cycles will be locked together. This signal is defined for locked cycles only. It is undefined for cycles which are not locked.
SMI#	I	The **system management interrupt** causes a system management interrupt request to be latched internally. When the latched SMI# is recognized on an instruction boundary, the processor enters System Management Mode.
SMIACT#	O	An active **system management interrupt active** output indicates that the processor is operating in System Management Mode.
STPCLK#	I	Assertion of the **stop clock** input signifies a request to stop the internal clock of the Pentium processor with MMX technology, thereby causing the core to consume less power. When the CPU recognizes STPCLK#, the processor will stop execution on the next instruction boundary, unless superseded by a higher priority interrupt, and generate a stop grant acknowledge cycle. When STPCLK# is asserted, the Pentium processor with MMX technology will still respond to interprocessor and external snoop requests.
TCK	I	The **testability clock** input provides the clocking function for the Pentium processor with MMX technology boundary scan in accordance with the IEEE Boundary Scan interface (Standard 1149.1). It is used to clock state information and data into and out of the Pentium processor with MMX technology during boundary scan.
TDI	I	The **test data input** is a serial input for the test logic. TAP instructions and data are shifted into the Pentium processor with MMX technology on the TDI pin on the rising edge of TCK when the TAP controller is in an appropriate state.
TDO	O	The **test data output** is a serial output of the test logic. TAP instructions and data are shifted out of the Pentium processor with MMX technology on the TDO pin on TCK's falling edge when the TAP controller is in an appropriate state.
TMS	I	The value of the **test mode select** input signal sampled at the rising edge of TCK controls the sequence of TAP controller state changes.
TRST#	I	When asserted, the **test reset** input allows the TAP controller to be asynchronously initialized.
V_{CC2}	I	The Pentium processor with MMX technology has 25 2.8V **power** inputs.
V_{CC3}	I	The Pentium processor with MMX technology has 28 3.3V **power** inputs.
V_{CC2}DET#	O	**V_{CC2} detect** is used in flexible motherboard implementations to configure the voltage output set-point appropriately for the V_{CC2} inputs of the processor.

Table 2. Quick Pin Reference (Cont'd)

Symbol	Type	Name and Function
V_{SS}	I	The Pentium processor with MMX technology has 53 **ground** inputs.
W/R#	O	**Write/read** is one of the primary bus cycle definition pins. It is driven valid in the same clock as the ADS# signal is asserted. W/R# distinguishes between write and read cycles.
WB/WT#	I	The **write back/write through** input allows a data cache line to be defined as write back or write through on a line-by-line basis. As a result, it determines whether a cache line is initially in the S or E state in the data cache.

Core and bus frequencies can be set according to Table 3 below. Each Pentium processor with MMX technology specified to operate within a single bus-to-core ratio and a specific minimum to maximum bus frequency range (corresponding to a minimum to maximum core frequency range). Operation in other bus-to-core ratios or outside the specified operating frequency range is not supported. For example, the 166 MHz Pentium processor with MMX technology does not operate beyond the 66 MHz bus frequency and only supports the 2/5 bus-to-core ratio; it does not support the 1/3, 1/2, or 2/3 bus-to-core ratios. Table 3 clarifies and summarizes these specifications.

Table 3. Bus Frequency Selections

BF1	BF0	Bus/Core Ratio	Max Bus/Core Frequency (MHz)	Min Bus/Core Frequency (MHz)
0	1	1/3	66/200	33/100
0	0	2/5	66/166	33/83
1	0	1/2 (1, 2)	N/A (2)	N/A (2)
1	1	2/7	66/233	33/117

NOTES:

1. This is the default bus to core ratio for the Pentium® processor with MMX™ technology. If the BF pins are left floating, the processor will be configured for the 1/2 bus to core frequency ratio.
2. Currently, there are no products that support these bus fractions.

2.4. Pin Reference Tables

Table 4. Output Pins

Name	Active Level	When Floated
ADS# (1)	Low	Bus Hold, BOFF#
ADSC#	Low	Bus Hold, BOFF#
APCHK#	Low	
BE7#-BE4#	Low	Bus Hold, BOFF#
BREQ	High	
CACHE# (1)	Low	Bus Hold, BOFF#
D/P# (2)	N/A	
FERR# (2)	Low	
HIT# (1)	Low	
HITM# (1, 3)	Low	
HLDA (1)	High	
IERR#	Low	
LOCK# (1)	Low	Bus Hold, BOFF#
M/IO# (1), D/C# (1), W/R# (1)	N/A	Bus Hold, BOFF#
PCHK#	Low	
BP3-2, PM1/BP1, PM0/BP0	High	
PRDY	High	
PWT, PCD	High	Bus Hold, BOFF#
SCYC (1)	High	Bus Hold, BOFF#
SMIACT#	Low	
TDO	N/A	All states except Shift-DR and Shift-IR
V_{CC}2DET#	Low	

NOTES:

All output and input/output pins are floated during tristate test mode (except IERR#).

1. These are I/O signals when two Pentium® processor with MMX™ technology are operating in dual processing mode.
2. These signals are undefined when the processor is configured as a Dual processor.
3. M# pin has an internal pull-up resistor.

Table 5. Input Pins

Name	Active Level	Synchronous/ Asynchronous	Internal Resistor	Qualified
A20M# (1)	Low	Asynchronous		
AHOLD	High	Synchronous		
APICEN	High	Synchronous/RESET	Pull-up	
BF0	N/A	Synchronous/RESET	Pull-down	
BF1	N/A	Synchronous/RESET	Pull-up	
BOFF#	Low	Synchronous		
BRDY#	Low	Synchronous	Pull-up	Bus State T2, T12, T2P
BRDYC#	Low	Synchronous	Pull-up	Bus State T2, T12, T2P
BUSCHK#	Low	Synchronous	Pull-up	BRDY#
CLK	N/A			
CPUTYP	High	Synchronous/RESET	Pull-down	
EADS#	Low	Synchronous		
EWBE#	Low	Synchronous		BRDY#
FLUSH#	Low	Asynchronous		
HOLD	High	Synchronous		
IGNNE# (1)	Low	Asynchronous		
INIT	High	Asynchronous		
INTR	High	Asynchronous		
INV	High	Synchronous		EADS#
LINT[1:0]	High	Asynchronous		APICEN at RESET
KEN#	Low	Synchronous		First BRDY#/NA#
NA#	Low	Synchronous		Bus State T2, TD, T2P
NMI	High	Asynchronous		
PEN#	Low	Synchronous		BRDY#
PICCLK	High	Asynchronous	Pull-up	
R/S#	N/A	Asynchronous	Pull-up	
RESET	High	Asynchronous		
SMI#	Low	Asynchronous	Pull-up	
STPCLK#	Low	Asynchronous	Pull-up	
TCK	N/A		Pull-up	
TDI	N/A	Synchronous/TCK	Pull-up	TCK
TMS	N/A	Synchronous/TCK	Pull-up	TCK
TRST#	Low	Asynchronous	Pull-up	
WB/WT#	N/A	Synchronous		First BRDY#/NA#

NOTES:

1. Undefined when the processor is configured as a Dual processor.

Table 6. Input/Output Pins (1)

Name	Active Level	When Floated	Qualified (when an input)	Internal Resistor
A31-A3	N/A	Address Hold, Bus Hold, BOFF#	EADS#	
AP	N/A	Address Hold, Bus Hold, BOFF#	EADS#	
BE3#-BE0#	Low	Address Hold, Bus Hold, BOFF#	RESET	Pull-down (2)
D63-D0	N/A	Bus Hold, BOFF#	BRDY#	
DP7-DP0	N/A	Bus Hold, BOFF#	BRDY#	
DPEN#	low		RESET	Pull-up
PICD0	N/A			Pull-up
PICD1	N/A			Pull-down

NOTES:

1. All output and input/output pins are floated during tristate test mode (except TDO, IERR# and TDO).
2. BE3#-BE0# have Pull-downs during RESET only.

Table 7. Inter-Processor Input/Output Pins

Name	Active Level	Internal Resistor
PHIT#	Low	Pull-up
PHITM#	Low	Pull-up
PBGNT#	Low	Pull-up
PBREQ#	Low	Pull-up

NOTES:

For proper inter-processor operation, the system cannot load these signals.

2.5. Pin Grouping According to Function

Table 8 organizes the pins with respect to their function.

Table 8. Pin Functional Grouping

Function	Pins
Clock	CLK
Initialization	RESET, INIT, BF1–BF0
Address Bus	A31-A3, BE7#–BE0#
Address Mask	A20M#
Data Bus	D63-D0
Address Parity	AP, APCHK#
APIC Support	PICCLK, PICD0-1
Data Parity	DP7-DP0, PCHK#, PEN#
Internal Parity Error	IERR#
System Error	BUSCHK#
Bus Cycle Definition	M/IO#, D/C#, W/R#, CACHE#, SCYC, LOCK#
Bus Control	ADS#, ADSC#, BRDY#, BRDYC#, NA#
Page Cacheability	PCD, PWT
Cache Control	KEN#, WB/WT#
Cache Snooping/Consistency	AHOLD, EADS#, HIT#, HITM#, INV
Cache Flush	FLUSH#
Write Ordering	EWBE#
Bus Arbitration	BOFF#, BREQ, HOLD, HLDA
Dual Processing Private Bus Control	PBGNT#, PBREQ#, PHIT#, PHITM#
Interrupts	INTR, NMI
Floating-Point Error Reporting	FERR#, IGNNE#
System Management Mode	SMI#, SMIACT#
TAP Port	TCK, TMS, TDI, TDO, TRST#
Breakpoint/Performance Monitoring	PM0/BP0, PM1/BP1, BP3-2
Power Management	STPCLK#
Miscellaneous Dual Processing	CPUTYP, D/P#
Debugging	R/S#, PRDY
Voltage Detection	VCC2DET#

3.0. ELECTRICAL SPECIFICATIONS

This section describes the electrical differences between the Pentium processor with MMX technology and the Pentium processor 133/150/166/200, as well as the AC and DC specifications of the Pentium processor with MMX technology.

3.1. Electrical Characteristics and Differences between the Pentium® Processor with MMX™ Technology and the Pentium Processor 133/150/166/200

When designing a Pentium processor with MMX technology system from a Pentium processor 133/150/166/200 system, there are a number of electrical differences that require attention. Designing a single motherboard that supports various members of the Pentium processor family including the Pentium processor with MMX technology, Pentium processor 133/150/166/200, Pentium OverDrive® processor, or future Pentium OverDrive processor can be easily accomplished. Refer to the *Pentium® Processor Flexible Motherboard Design Guidelines* application note (Order Number 243187) for more information and specific implementation examples.

The following sections highlight key electrical issues pertaining to the Pentium processor with MMX technology power supplies, connection specifications and buffer models.

3.1.1. POWER SUPPLIES

The main electrical difference between the Pentium processor with MMX technology and the Pentium processor 133/150/166/200 is the operating voltage. The Pentium processor with MMX technology requires two separate voltage inputs, V_{CC2} and V_{CC3}. The V_{CC2} pins supply power to the Pentium processor with MMX technology core, while the V_{CC3} pins supply power to the processor I/O pins.

The Pentium processor 133/150/166/200, on the other hand, requires a single voltage supply for all V_{CC} pins. This single supply powers both the core and I/O pins of the Pentium processor 133/150/166/200.

By connecting all of the V_{CC2} pins together and all the V_{CC3} pins together on separate power islands, Pentium processor 133/150/166/200 designs can easily be converted to support the Pentium processor with MMX technology. In order to maintain compatibility with Pentium processor 133/150/166/200-based platforms, the Pentium processor with MMX technology supports the standard 3.3V specification on its V_{CC3} pins.

3.1.1.1. Power Supply Sequencing

There is no specific power sequence required for powering up or powering down the separate V_{CC2} and V_{CC3} supplies of the Pentium processor with MMX technology. It is recommended that the V_{CC2} and V_{CC3} supplies be either both ON or both OFF within one second of each other.

3.1.2. CONNECTION SPECIFICATIONS

Connection specifications for the power and ground inputs, 3.3V inputs and outputs, and the NC/INC and unused inputs are discussed in the following sections.

3.1.2.1. Power and Ground

For clean on-chip power distribution, the Pentium processor with MMX technology in PPGA and SPGA packages has 28 V_{CC3} (I/O power), 25 V_{CC2} (core power) and 53 V_{SS} (ground) inputs. Power and ground connections must be made to all external V_{CC} and V_{SS} pins of the Pentium processor with MMX technology. On the circuit board all V_{CC3} pins must be connected to a 3.3V V_{CC} plane. All V_{CC2} pins must be connected to a 2.8V V_{CC} plane. All V_{SS} pins must be connected to a V_{SS} plane.

3.1.2.1.1. V_{CC2} and V_{CC3} Measurement Specification

The values of V_{CC2} and V_{CC3} should be measured at the bottom side of the processor pins using an oscilloscope with a 3 dB bandwidth of at least 20 MHz (100 MS/s digital sampling rate). There should be a short isolation ground lead attached to a processor pin on the bottom side of the board.

The measurement should be taken at the following V_{CC}/V_{SS} pairs: AN13/AM10, AN21/AM18, AN29/AM26, AC37/Z36, U37/R36, L37/H36, A25/B28, A17/B20, A7/B10, G1/K2, S1/V2, AC1/Z2. One-half of these pins are V_{CC2} while the others are V_{CC3}; the operating ranges for the V_{CC2} and V_{CC3} pins are

specified at different voltages. See Table 10 for the specification.

The display should show continuous sampling of the voltage line, at 20 mV/div, and 500 ns/div with the trigger point set to the center point of the range. Slowly move the trigger to the high and low ends of the specification, and verify that excursions beyond these limits are not observed. There are no allowances for crossing the high and low limits of the voltage specification. For more information on measurement techniques, see the *Voltage Guidelines for Pentium® Processors with MMX™ Technology* application note (Order Number 243186).

3.1.2.1.2. Decoupling Recommendations

Liberal decoupling capacitance should be placed near the Pentium processor with MMX technology. The Pentium processor with MMX technology, when driving its large address and data buses at high frequencies, can cause transient power surges, particularly when driving large capacitive loads.

Low inductance capacitors and interconnects are recommended for best high frequency electrical performance. Inductance can be reduced by shortening circuit board traces between the Pentium processor with MMX technology and decoupling capacitors as much as possible. These capacitors should be evenly distributed around each component on the power plane. Capacitor values should be chosen to ensure they eliminate both low and high frequency noise components.

For the Pentium processor with MMX technology, the power consumption can transition from a low level of power to a much higher level (or high to low power) very rapidly. A typical example would be entering or exiting the Stop Grant State. Another example would be executing a HALT instruction, causing the Pentium processor with MMX technology to enter the AutoHALT Power Down State, or transitioning from HALT to the Normal State. All of these examples may cause abrupt changes in the power being consumed by the Pentium processor with MMX technology. Note that the AutoHALT Power Down feature is always enabled even when other power management features are not implemented.

Bulk storage capacitors with a low Effective Series Resistance (ESR) in the 10Ω to 100Ω range are required to maintain a regulated supply voltage during the interval between the time the current load changes and the point that the regulated power supply output can react to the change in load. In order to reduce the ESR, it may be necessary to place several bulk storage capacitors in parallel.

These capacitors should be placed near the Pentium processor with MMX technology on both the V_{CC2} and V_{CC3} plane to ensure that the supply voltage stays within specified limits during changes in the supply current during operation.

Detailed decoupling recommendations are provided in the Flexible Motherboard Design Guidelines application note (Order Number 243187)

3.1.2.2. 3.3V Inputs and Outputs

The inputs and outputs of the Pentium processor with MMX technology comply with the 3.3V JEDEC standard levels. Both inputs and outputs are also TTL-compatible, although the inputs cannot tolerate voltage swings above the V_{IN3} (max) specification.

System support components which use TTL-compatible inputs will interface to the Pentium processor with MMX technology without extra logic. This is because the Pentium processor drives according to the 5V TTL specification (but not beyond 3.3V).

For Pentium processor with MMX technology inputs, the voltage must not exceed the 3.3V V_{IN3} (max) specification. System support components can consist of 3.3V devices or open-collector devices. In an open-collector configuration, the external resistor should be biased to V_{CC3}.

All pins, including the CLK and PICCLK of the Pentium processor with MMX technology, are 3.3V-tolerant-only. If an 8259A interrupt controller is used, for example, the system must provide level converters between the 8259A and the Pentium processor with MMX technology.

3.1.2.3. NC/INC and Unused Inputs

All NC and INC pins must remain unconnected.

For reliable operation, always connect unused inputs to an appropriate signal level. Unused active low inputs should be connected to V_{CC3}. Unused active high inputs should be connected to V_{SS} (ground).

3.1.2.4. Private Bus

When two Pentium processors with MMX technology are operating in dual processor mode, a "private bus" exists to arbitrate for the processor bus and maintain local cache coherency. The private bus consists of two pinout changes:

1. Five pins are added: PBREQ#, PBGNT#, PHIT#, PHITM#, D/P#.
2. Ten output pins become I/O pins: ADS#, D/C#, W/R#, M/IO#, CACHE#, LOCK#, HIT#, HITM#, HLDA, SCYC, BE#4.

The new pins are given AC specifications of valid delays at 0 pF, setup times and hold times. Simulate with these parameters and their respective I/O buffer models to guarantee that proper timings are met.

The AC specification gives input setup and hold times for the ten signals that become I/O pins. These setup and hold times must only be met when a dual processor is present in the system.

3.1.3. BUFFER MODELS

The structure of the buffer models for the Pentium processor with MMX technology and the Pentium processor 133/150/166/200 are identical. Some of the values of the components have changed to reflect the minor manufacturing process and package differences between the processors. The system should see insignificant differences between the AC behavior of the Pentium processor with MMX technology and the Pentium processor 133/150/166/200.

Simulation of AC timings using the Pentium processor with MMX technology buffer models is recommended to ensure robust system designs. Pay specific attention to the signal quality restrictions imposed by 3.3V buffers.

3.2. Absolute Maximum Ratings

Table 9 provides stress ratings only. Functional operation at the Absolute Maximum Ratings is not implied or guaranteed. Functional operating conditions are given in the AC and DC specification tables.

Extended exposure to the maximum ratings may affect device reliability. Furthermore, although the Pentium processor with MMX technology contains protective circuitry to resist damage from electrostatic discharge, always take precautions to avoid high static voltages or electric fields.

Table 9. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes
	Storage Temperature	–65	150	°C	
	Case Temperature Under Bias	–65	110	°C	
V_{CC3}	V_{CC3} Supply Voltage with respect to V_{SS}	–0.5	4.6	V	
V_{CC2}	V_{CC2} Supply Voltage with respect to V_{SS}	–0.5	3.7	V	
V_{IN3}	3V Only Buffer DC Input Voltage	–0.5	V_{CC3} +0.5 (not to exceed V_{CC3} max)	V	

WARNING

Stressing the device beyond the Absolute Maximum Ratings may cause permanent damage. These are stress ratings only. Operation beyond the DC specifications is not recommended or guaranteed and extended exposure beyond the DC specifications may affect device reliability.

3.3. DC Specifications

Table 10 and Table 11 list the DC Specifications of the Pentium processor with MMX technology.

Table 10. V_{CC} and T_{CASE} Specifications

Symbol	Parameter	Min	Nom	Max	Unit	Notes
T_{CASE}	Case Temperature	0		70	°C	
V_{CC2}	V_{CC2} Voltage	2.7	2.8	2.9	V	Range = 2.8 ± 3.57% (1)
V_{CC3}	V_{CC3} Voltage	3.135	3.3	3.6	V	Range = 3.3 –5%, +9.09% (1)

NOTES:

1. See the V_{CC} measurement specification section earlier in this chapter.

Table 11. 3.3V DC Specifications
(See Table 10 for V_{CC} and T_{CASE} assumptions.)

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL3}	Input Low Voltage	–0.3	0.8	V	TTL Level
V_{IH3}	Input High Voltage	2.0	V_{CC3} +0.3	V	TTL Level (3)
V_{OL3}	Output Low Voltage		0.4	V	TTL Level (1, 4)
V_{OH3}	Output High Voltage	2.4		V	TTL Level (2)

NOTES:

1. Parameter measured at –4 mA.
2. Parameter measured at 3 mA.
3. Parameter measured at nominal V_{CC3} which is 3.3V.
4. In dual processing systems, up to a 10 mA load from the second processor may be observed on the PCHK# signal. Based on silicon characterization data, V_{OL3} of PCHK# will remain less than 400 mV even with a 10 mA load. PCHK# V_{OL3} will increase to approximately 500 mV with a 14 mA load (worst case for a DP system with a 4 mA system load).

Table 12. I_{CC} Specifications
(Measured at V_{CC2}=2.9V and V_{CC3}=3.6V.)

Symbol	Parameter	Min	Max	Unit	Notes
I_{CC2}	Power Supply Current		6500 5700 4750	mA mA mA	233 MHz 200 Mhz (1) 166 MHz (1)
I_{CC3}	Power Supply Current		750 650 540	mA mA mA	233 MHz 200 MHz (1) 166 MHz (1)

NOTES:

1. This value should be used for power supply design. It was determined using a worst case instruction mix and maximum V_{CC}. Power supply transient response and decoupling capacitors must be sufficient to handle the instantaneous current changes occurring during transitions from Stop Clock to full Active modes.

Table 13. Power Dissipation Requirements for Thermal Design
(Measured at V_{CC2}=2.8V and V_{CC3}=3.3V.)

Parameter	Typical [1]	Max [2]	Unit	Notes
Active Power	7.9 (5) 7.3 (5) 6.1 (5)	17.0 (6) 15.7 (6) 13.1 (6)	Watts Watts Watts	233 MHz 200 MHz 166 MHz
Stop Grant / Auto Halt Powerdown Power		2.61 2.41 2.05	Watts Watts Watts	233 MHz (3) 200 MHz (3) 166 MHz (3)
Stop Clock Power	0.03	< 0.3	Watts	All frequencies [4]

NOTES:

1. This is the typical power dissipation in a system. This value is expected to be the average value that will be measured in a system using a typical device at V_{CC2} = 2.8V running typical applications. This value is highly dependent upon the specific system configuration. Typical power specifications are not tested.
2. Systems must be designed to thermally dissipate the maximum active power dissipation. It is determined using worst case instruction mix with V_{CC2} = 2.8V and V_{CC3} = 3.3 and also takes into account the thermal time constants of the package.
3. Stop Grant/Auto Halt Power Down Power Dissipation is determined by asserting the STPCLK# pin or executing the HALT instruction.
4. Stop Clock Power Dissipation is determined by asserting the STPCLK# pin and then removing the external CLK input.
5. Active Power (typ) is the average power measured in a system using a typical device running typical applications under normal operating conditions at nominal V_{CC} and room temperature.
6. Active Power (max) is the maximum power dissipation under normal operating conditions at nominal V_{CC2}, worst-case temperature, while executing the worst case power instruction mix. Active power (max) is equivalent to Thermal Design Power (max).

Table 14. Input and Output Characteristics

Symbol	Parameter	Min	Max	Unit	Notes
C_{IN}	Input Capacitance		15	pF	(4)
C_O	Output Capacitance		20	pF	(4)
$C_{I/O}$	I/O Capacitance		25	pF	(4)
C_{CLK}	CLK Input Capacitance		15	pF	(4)
C_{TIN}	Test Input Capacitance		15	pF	(4)
C_{TOUT}	Test Output Capacitance		20	pF	(4)
C_{TCK}	Test Clock Capacitance		15	pF	(4)
I_{LI}	Input Leakage Current		±15	µA	$0 < V_{IN} < V_{IL}$, $V_{IH} > V_{IN} > V_{CC}$ (1)
I_{LO}	Output Leakage Current		±15	µA	$0 < V_{IN} < V_{IL}$, $V_{IH} > V_{IN} > V_{CC}$ (1)
I_{IH}	Input Leakage Current		200	µA	$V_{IN} = 2.4V$ (3)
I_{IL}	Input Leakage Current		–400	µA	$V_{IN} = 0.4V$ (2, 5)

NOTES:

1. This parameter is for inputs/outputs without an internal pull-up or pull-down.
2. This parameter is for inputs with an internal pull-up.
3. This parameter is for inputs with an internal pull-down.
4. Guaranteed by design.
5. This specification applies to the HITM# pin when it is driven as an input (e.g., in JTAG mode).

3.4. AC Specifications

The AC specifications consist of output delays, input setup requirements and input hold requirements. All AC specifications (with the exception of those for the TAP signals and APIC signals) are relative to the rising edge of the CLK input.

All timings are referenced to 1.5 volts for both "0" and "1" logic levels unless otherwise specified. Within the sampling window, a synchronous input must be stable for correct Pentium processor with MMX technology operation.

Each valid delay is specified for a 0 pF load. The system designer should use I/O buffer modeling to account for signal flight time delays.

Each Pentium processor with MMX technology specified to operate within a single bus-to-core ratio and a specific minimum to maximum bus frequency range (corresponding to a minimum to maximum core frequency range). Operation in other bus-to-core ratios or outside the specified operating frequency range is not supported. For example, the 166 MHz Pentium processor with MMX technology does not operate beyond the 66 MHz bus frequency and only supports the 2/5 bus-to-core ratio; it does not support the 1/3, 1/2, or 2/3 bus-to-core ratios. Table 3 clarifies and summarizes these specifications.

Table 15. Pentium® Processor with MMX™ Technology AC Specifications for 66-MHz Bus Operation

(See Table 10 for V_{CC} and T_{CASE} specifications, C_L = 0 pF.)

Symbol	Parameter	Min	Max	Unit	Figure	Notes
	Frequency	33.33	66.6	MHz	4	
t_{1a}	CLK Period	15.0	30.0	ns	4	
t_{1b}	CLK Period Stability		±250	ps		Adjacent Clocks (1, 25)
t_2	CLK High Time	4.0		ns	4	2V (1)
t_3	CLK Low Time	4.0		ns	4	0.8V (1)
t_4	CLK Fall Time	0.15	1.5	ns	4	(2.0V–0.8V) (1, 5)
t_5	CLK Rise Time	0.15	1.5	ns	4	(0.8V–2.0V) (1, 5)
t_{6a}	PWT, PCD, CACHE# Valid Delay	1.0	7.0	ns	5	
t_{6b}	AP Valid Delay	1.0	8.5	ns	5	
t_{6c}	BE0-7#, LOCK# Valid Delay	0.9	7.0	ns	5	(4)
t_{6d}	ADS# Valid Delay	0.8	6.0	ns	5	
t_{6e}	ADSC#, D/C#, W/R#, SCYC, Valid Delay	0.8	7.0	ns	5	
t_{6f}	M/IO# Valid Delay	0.8	5.9	ns	5	
t_{6g}	A3–A16 Valid Delay	0.5	6.6	ns	5	
t_{6h}	A17–A31 Valid Delay	0.6	6.6	ns	5	

Table 15. Pentium® Processor with MMX™ Technology AC Specifications for 66-MHz Bus Operation (Cont'd)

(See Table 10 for V_{CC} and T_{CASE} specifications, C_L = 0 pF.)

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_7	ADS#, ADSC#, AP, A3-A31, PWT, PCD, BE0-7#, M/IO#, D/C#, W/R#, CACHE#, SCYC, LOCK# Float Delay		10.0	ns	6	(1)
t_{8a}	APCHK#, IERR#, FERR# Valid Delay	1.0	8.3	ns	5	(4)
t_{8b}	PCHK# Valid Delay	1.0	7.0	ns	5	(4)
t_{9a}	BREQ Valid Delay	1.0	8.0	ns	5	(4)
t_{9b}	SMIACT# Valid Delay	1.0	7.3	ns	5	(4)
t_{9c}	HLDA Valid Delay	1.0	6.8	ns	5	
t_{10a}	HIT# Valid Delay	1.0	6.8	ns	5	
t_{10b}	HITM# Valid Delay	0.7	6.0	ns	5	
t_{11a}	PM0-1, BP0-3 Valid Delay	1.0	10.0	ns	5	
t_{11b}	PRDY Valid Delay	1.0	8.0	ns	5	
t_{12}	D0-D63, DP0-7 Write Data Valid Delay	1.3	7.5	ns	5	
t_{13}	D0-D63, DP0-3 Write Data Float Delay		10.0	ns	6	(1)
t_{14}	A5-A31 Setup Time	6.0		ns	7	(26)
t_{15}	A5-A31 Hold Time	1.0		ns	7	
t_{16a}	INV, AP Setup Time	5.0		ns	7	
t_{16b}	EADS# Setup Time	5.0		ns	7	
t_{17}	EADS#, INV, AP Hold Time	1.0		ns	7	
t_{18a}	KEN# Setup Time	5.0		ns	7	
t_{18b}	NA#, WB/WT# Setup Time	4.5		ns	7	
t_{19}	KEN#, WB/WT#, NA# Hold Time	1.0		ns	7	
t_{20}	BRDY#, BRDYC# Setup Time	5.0		ns	7	
t_{21}	BRDY#, BRDYC# Hold Time	1.0		ns	7	
t_{22}	AHOLD, BOFF# Setup Time	5.5		ns	7	
t_{23}	AHOLD, BOFF# Hold Time	1.0		ns	7	
t_{24a}	BUSCHK#, EWBE#, HOLD Setup Time	5.0		ns	7	

Table 15. Pentium® Processor with MMX™ Technology AC Specifications for 66-MHz Bus Operation (Cont'd)
(See Table 10 for V_{CC} and T_{CASE} specifications, C_L = 0 pF.)

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_{24b}	PEN# Setup Time	4.8		ns	7	
t_{25a}	BUSCHK#, EWBE#, PEN# Hold Time	1.0		ns	7	
t_{25b}	HOLD Hold Time	1.5		ns	7	
t_{26}	A20M#, INTR, STPCLK# Setup Time	5.0		ns	7	(12, 16)
t_{27}	A20M#, INTR, STPCLK# Hold Time	1.0		ns	7	(13)
t_{28}	INIT, FLUSH#, NMI, SMI#, IGNNE# Setup Time	5.0		ns	7	(12, 16, 17)
t_{29}	INIT, FLUSH#, NMI, SMI#, IGNNE# Hold Time	1.0		ns	7	(13)
t_{30}	INIT, FLUSH#, NMI, SMI#, IGNNE# Pulse Width, Async	2.0		CLK		(15, 17)
t_{31}	R/S# Setup Time	5.0		ns	7	(12, 16, 17)
t_{32}	R/S# Hold Time	1.0		ns	7	(13)
t_{33}	R/S# Pulse Width, Async.	2.0		CLK		15, 17)
t_{34}	D0-D63, DP0-7 Read Data Setup Time	2.8		ns	7	
t_{35}	D0-D63, DP0-7 Read Data Hold Time	1.5		ns	7	
t_{36}	RESET Setup Time	5.0		ns	8	(12, 16)
t_{37}	RESET Hold Time	1.0		ns	8	(13)
t_{38}	RESET Pulse Width, V_{CC} & CLK Stable	15.0		CLK	8	(17)
t_{39}	RESET Active After V_{CC} & CLK Stable	1.0		ms	8	Power up
t_{40}	Reset Configuration Signals (INIT, FLUSH#) Setup Time	5.0		ns	8	(12, 16, 17)
t_{41}	Reset Configuration Signals (INIT, FLUSH#) Hold Time	1.0		ns	8	(13)
t_{42a}	Reset Configuration Signals (INIT, FLUSH#) Setup Time, Async.	2.0		CLK		To RESET falling edge (16)
t_{42b}	Reset Configuration Signals	2.0		CLK		To RESET falling edge

Table 15. Pentium® Processor with MMX™ Technology AC Specifications for 66-MHz Bus Operation (Cont'd)

(See Table 10 for V_{CC} and T_{CASE} specifications, C_L = 0 pF.)

Symbol	Parameter	Min	Max	Unit	Figure	Notes
	(INIT, FLUSH#, BRDYC#, BUSCHK#) Hold Time, Async.					(27)
t_{42c}	Reset Configuration Signals (BRDYC#, BUSCHK#) Setup Time, Async.	3.0		CLK		To RESET falling edge (27)
t_{43a}	BF0, BF1, CPUTYP Setup Time	1.0		ms	8	To RESET falling edge (22)
t_{43b}	BF0, BF1, CPUTYP Hold Time	2.0		CLK		To RESET falling edge (22)
t_{43c}	APICEN, BE4# Setup Time	2.0		CLK		To RESET falling edge
t_{43d}	APICEN, BE4# Hold Time	2.0		CLK		To RESET falling edge
t_{44}	TCK Frequency		16.0	MHz		
t_{45}	TCK Period	62.5		ns	4	
t_{46}	TCK High Time	25.0		ns	4	2V (1)
t_{47}	TCK Low Time	25.0		ns	4	0.8V (1)
t_{48}	TCK Fall Time		5.0	ns	4	(2.0V–0.8V) (1, 8, 9)
t_{49}	TCK Rise Time		5.0	ns	4	(0.8V–2.0V) (1, 8, 9)
t_{50}	TRST# Pulse Width	40.0		ns	10	Asynchronous (1)
t_{51}	TDI, TMS Setup Time	5.0		ns	9	(7)
t_{52}	TDI, TMS Hold Time	13.0		ns	9	(7)
t_{53}	TDO Valid Delay	2.5	20.0	ns	9	(8)
t_{54}	TDO Float Delay		25.0	ns	9	(1, 8)
t_{55}	All Non-Test Outputs Valid Delay	2.5	20.0	ns	9	(3, 8, 10)
t_{56}	All Non-Test Outputs Float Delay		25.0	ns	9	(1, 3, 8, 10)
t_{57}	All Non-Test Inputs Setup Time	5.0		ns	9	(3, 7, 10)
t_{58}	All Non-Test Inputs Hold Time	13.0		ns	9	(3, 7, 10)
APIC AC Specifications						
t_{60a}	PICCLK Frequency	2.0	16.66	MHz	4	
t_{60b}	PICCLK Period	60.0	500.0	ns	4	
t_{60c}	PICCLK High Time	15.0		ns	4	
t_{60d}	PICCLK Low Time	15.0		ns	4	

Table 15. Pentium® Processor with MMX™ Technology AC Specifications for 66-MHz Bus Operation (Cont'd)
(See Table 10 for V_{CC} and T_{CASE} specifications, C_L = 0 pF.)

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_{60e}	PICCLK Rise Time	0.15	2.5	ns	4	
t_{60f}	PICCLK Fall Time	0.15	2.5	ns	4	
t_{60g}	PICD0-1 Setup Time	3.0		ns	7	To PICCLK
t_{60h}	PICD0-1 Hold Time	2.5		ns	7	To PICCLK
t_{60i}	PICD0-1 Valid Delay (LtoH)	4.0	38.0	ns	5	From PICCLK (28)
t_{60j}	PICD0-1 Valid Delay (HtoL)	4.0	22.0	ns	5	From PICCLK (28)

NOTES:
Please refer to Table 16 for footnotes.

Table 16. Pentium® Processor with MMX™ Technology Dual Processor Mode AC Specifications for 66-MHz Bus Operation
(See Table 10 for V_{CC} and T_{CASE} assumptions.)

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_{80a}	PBREQ#, PBGNT#, PHIT# Flight Time	0.0	2.0	ns	5	(11, 24)
t_{80b}	PHITM# Flight Time	0.0	1.8	ns	5	(11, 24)
t_{83a}	A5-A31 Setup Time	3.7		ns	7	(18)
t_{83b}	D/C#, W/R#, CACHE#, LOCK#, SCYC Setup Time	4.0		ns	7	(18, 21)
t_{83c}	ADS#, M/IO# Setup Time	5.8		ns	7	(18, 21)
t_{83d}	HIT#, HITM# Setup Time	6.0		ns	7	(18, 21)
t_{83e}	HLDA Setup Time	6.0		ns	7	(18, 21)
t_{84a}	CACHE#, HIT# Hold Time	1.0		ns	7	(18, 21)
t_{84b}	ADS#, D/C#, W/R#, M/IO#, A5-A31, HLDA, SCYC Hold Time	0.8		ns	7	(18, 21)
t_{84c}	LOCK# Hold Time	0.9		ns	7	(18, 21)
t_{84d}	HITM# Hold Time	0.7		ns	7	(18, 21)
t_{85}	DPEN# Valid Time		10.0	CLK		(18, 19, 23)
t_{86}	DPEN# Hold Time	2.0		CLK		(18, 20, 23)
t_{87}	APIC ID (BE0#-BE3#) Setup Time	2.0		CLK	8	To falling Edge of RESET (23)
t_{88}	APIC ID (BE0#-BE3#) Hold Time	2.0		CLK	8	From Falling Edge of RESET (23)
t_{89}	D/P# Valid Delay	1.0	8.0	ns	5	Primary Processor Only

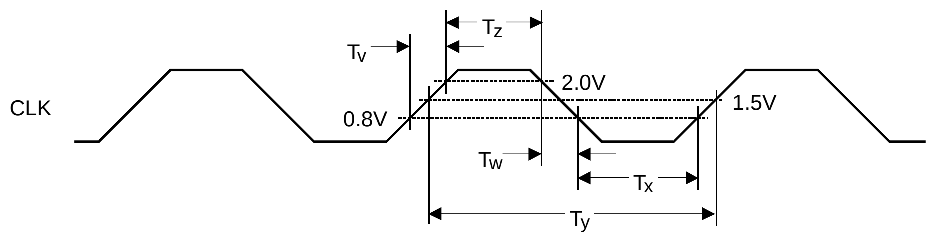
NOTES:

Notes 2, 6 and 14 are general and apply to all standard TTL signals used with the Pentium® processor family.

Each valid delay is specified for a 0 pF load. The system designer should use I/O buffer models to account for signal flight time delays.

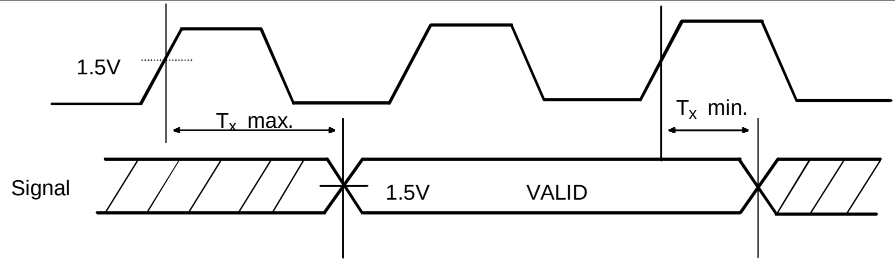
1. Not 100% tested. Guaranteed by design/characterization.
2. TTL input test waveforms are assumed to be 0 to 3V transitions with 1 V/ns rise and fall times.
3. Non-test outputs and inputs are the normal output or input signals (besides TCK, TRST#, TDI, TDO and TMS). These timings correspond to the response of these signals due to boundary scan operations.
4. APCHK#, FERR#, HLDA, IERR#, LOCK# and PCHK# are glitch-free outputs. Glitch-free signals monotonically transition without false transitions (i.e., glitches).
5. 0.8V/ns (CLK input rise/fall time $\leq$ 8V/ns.
6. 0.3V/ns (input rise/fall time $\leq$ 5V/ns.
7. Referenced to TCK rising edge.
8. Referenced to TCK falling edge.
9. 1 ns can be added to the maximum TCK rise and fall times for every 10 MHz of frequency below 33 MHz.
10. During debugging, do not use the boundary scan timings (t_{55} to t_{58}).

11. This is a flight time specification, that includes both flight time and clock skew. The flight time is the time from where the unloaded driver crosses 1.5V (50% of min V_{CC}), to where the receiver crosses the 1.5V level (50% of min V_{CC}). See Figure 11. The minimum flight time minus the clock skew must be greater than zero.
12. Setup time is required to guarantee recognition on a specific clock. Pentium processor with MMX™ technology must meet this specification for dual processor operation for the FLUSH# and RESET signals.
13. Hold time is required to guarantee recognition on a specific clock. Pentium processor with MMX technology must meet this specification for dual processor operation for the FLUSH# and RESET signals.
14. All TTL timings are referenced from 1.5V.
15. To guarantee proper asynchronous recognition, the signal must have been de-asserted (inactive) for a minimum of two clocks before being returned active and must meet the minimum pulse width.
16. This input may be driven asynchronously. However, when operating two processors in dual processing mode, FLUSH# and RESET must be asserted synchronously to both processors.
17. When driven asynchronously, RESET, NMI, FLUSH#, R/S#, INIT and SMI# must be de-asserted (inactive) for a minimum of two clocks before being returned active.
18. Timings are valid only when dual processor is present.
19. Maximum time DPEN# is valid from rising edge of RESET.
20. Minimum time DPEN# is valid after falling edge of RESET.
21. The D/C#, M/IO#, W/R#, CACHE# and A5–A31 signals are sampled only on the CLK that ADS# is active.
22. In order to override the internal defaults and guarantee that the BF[1:0] inputs remain stable while RESET is active, these pins should be strapped directly to or through a pull-up/pull-down resistor to V_{CC3} or ground. Driving these pins with active logic is not recommended unless stability duringt RESET can be guaranteed. Similarly, CPUTYP should also be strapped directly to or through a pull-up/pull-down resistor to V_{CC3} or ground.
23. RESET is synchronous in dual processing mode. All signals which have a setup or hold time with respect to a falling or rising edge of RESET in UP mode, should be measured with respect to the first processor clock edge in which RESET is sampled either active or inactive in dual processing mode.
24. The PHIT# and PHITM# signals operate at the core frequency.
25. These signals are measured on the rising edge of adjacent CLKs at 1.5V. To ensure a 1:1 relationship between the amplitude of the input jitter and the internal and external clocks, the jitter frequency spectrum should not have any power spectrum peaking between 500 kHz and 1/3 of the CLK operating frequency. The amount of jitter present must be accounted for as a component of CLK skew between devices. The internal clock generator requires a constant frequency CLK input to within ±250 ps. Therefore, the CLK input cannot be changed dynamically.
26. In dual processing mode, timing t14 is replaced by t_{83a}. Timing t_{14} is required for external snooping (e.g., address setup to the CLK in which EADS# is sampled active) in both uniprocessor and dual processor modes.
27. BRDYC# and BUSCHK# are used as reset configuration signals to select buffer size.
28. This assumes an external pull-up resistor to V_{CC} and a lumped capacitive load. The pull-up resistor must be between 300 ohms and 1K ohms, the capacitance must be between 20 pF and 240 pF, and the RC product must be between 6 ns and 36 ns. VOL for PICD0-1 is 0.55V.



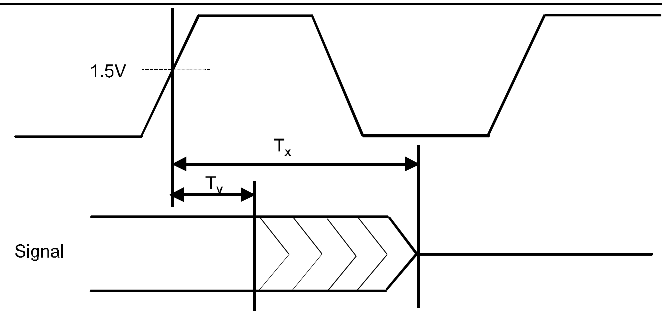
Tv = t5, t49, t60e
Tw = t4, t48, t60f
Tx = t3, t47, t60d
Ty = t1, t45, t60b
Tz = t2, t46, t60c

Figure 4. Clock Waveform



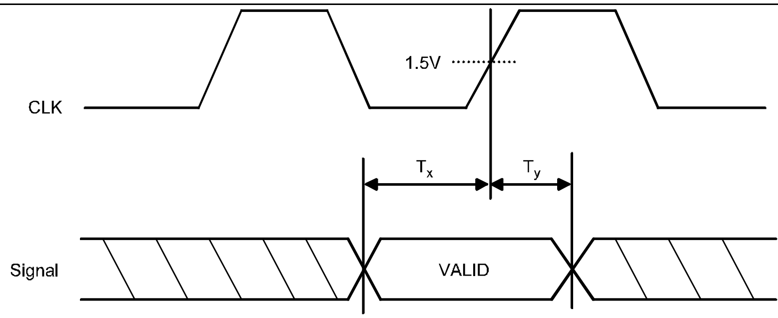
Tx = t6, t8, t9, t10, t11, t12, t60i, t60j, t80a, t89

Figure 5. Valid Delay Timings



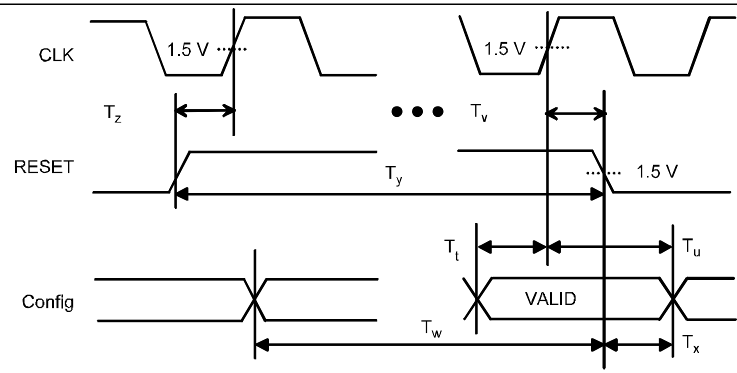
Tx = t7, t13; Ty = t6min, t12min

Figure 6. Float Delay Timings



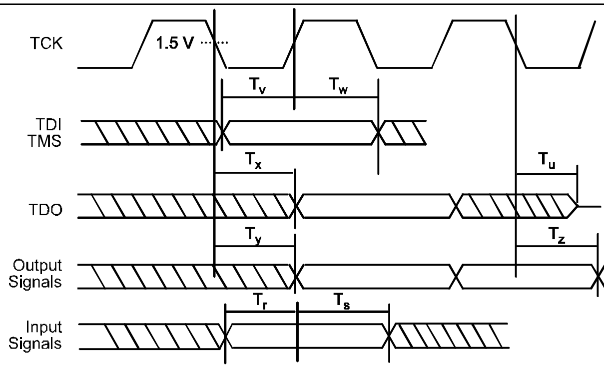
Tx = t14, t16, t18, t20, t22, t24, t26, t28, t31, t34, t60g (to PICCLK),t81, t83
Ty = t15, t17, t19, t21, t23, t25, t27, t29, t32, t35, t60h (to PICCLK), t82, t84

Figure 7. Setup and Hold Timings



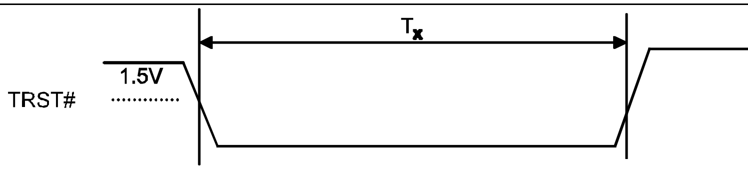
Tt = t40, Tu = t41, Tv = t37, T w =t42, t43a, t43c, t87, Tx = t43b, t43d, t43f, t88, Ty = t38, t39, Tz = t36

Figure 8. Reset and Configuration Timings



Tr = t57, Ts = t58, Tu = t54, Tv = t51, Tw = t52, Tx = t53, Ty = t55, Tz = t56

Figure 9. Test Timings



Tx = t50

Figure 10. Test Reset Timings

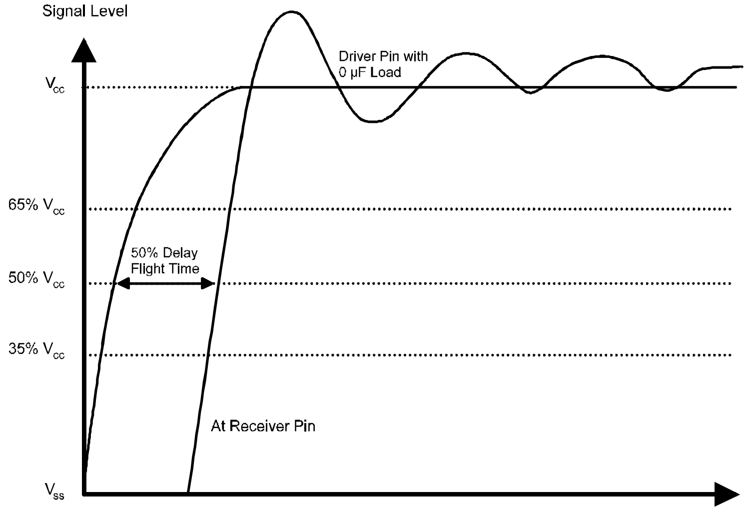


Figure 11. 50 Percent V_{CC} Measurement of Flight Time

4.0. MECHANICAL SPECIFICATIONS

The Pentium processor with MMX technology is packaged in 296-pin staggered pin grid array ceramic (SPGA) or plastic (PPGA) packages. The pins are arranged in a 37 x 37 matrix and the package dimensions are 1.95" x 1.95" (Table 17). A 1.25" x 1.25" copper tungsten heat spreader may be attached to the top of some of the ceramic packages. This package design with spreader has been replaced with a package which has no attached spreader. In this section, both ceramic (spreader and non-spreader) as well as plastic packages are shown.

Package summary information is provided in Table 17. The mechanical specifications for the Pentium processor with MMX technology are provided in Table 18 and Table 19. Figure 12 and Figure 13 show the package dimensions.

Table 17. Package Information Summary for Pentium® Processor with MMX™ Technologty

Package Type	Total Pins	Pin Array	Package Size
Ceramic Staggered Pin Grid Array (SPGA)	296	37 x 37	1.95" x 1.95" 4.95 cm x 4.95 cm
Plastic Staggered Pin Grid Array (PPGA)	296	37 x 37	1.95" x 1.95" 4.95 cm x 4.95 cm

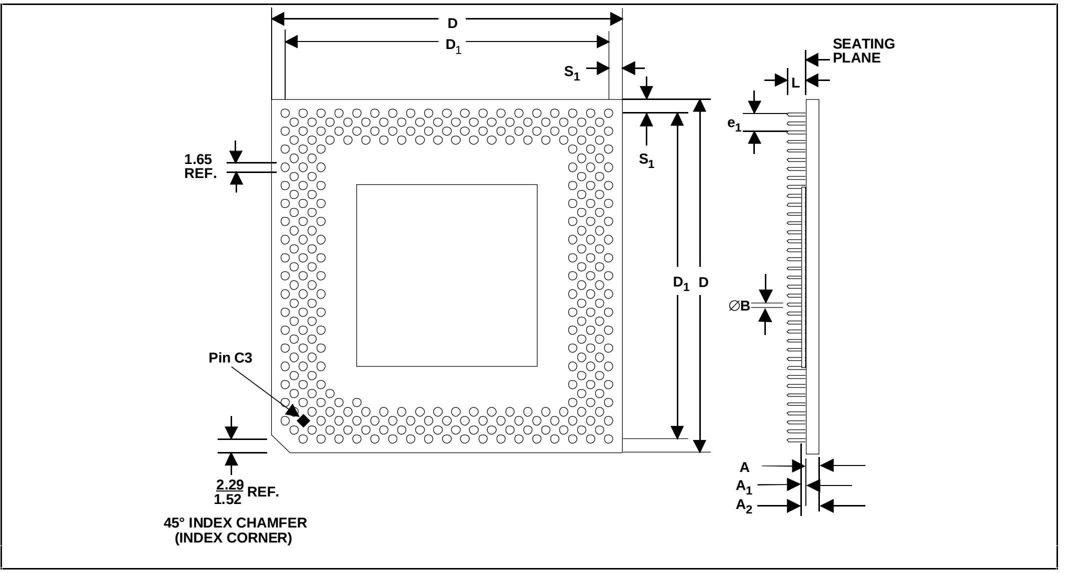


Figure 12. SPGA Package Dimensions

Table 18. SPGA Package Dimensions

Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
A	2.62	2.97		0.103	0.117	
A_1	0.69	0.84	Ceramic Lid	0.027	0.033	Ceramic Lid
A_2	3.31	3.81	Ceramic Lid	0.130	0.150	Ceramic Lid
B	0.43	0.51		0.017	0.020	
D	49.28	49.78		1.940	1.960	
D_1	45.59	45.85		1.795	1.805	
e_1	2.29	2.79		0.090	0.110	
L	3.05	3.30		0.120	0.130	
N	296		Lead Count	296		Lead Count
S_1	1.52	2.54		0.060	0.100	

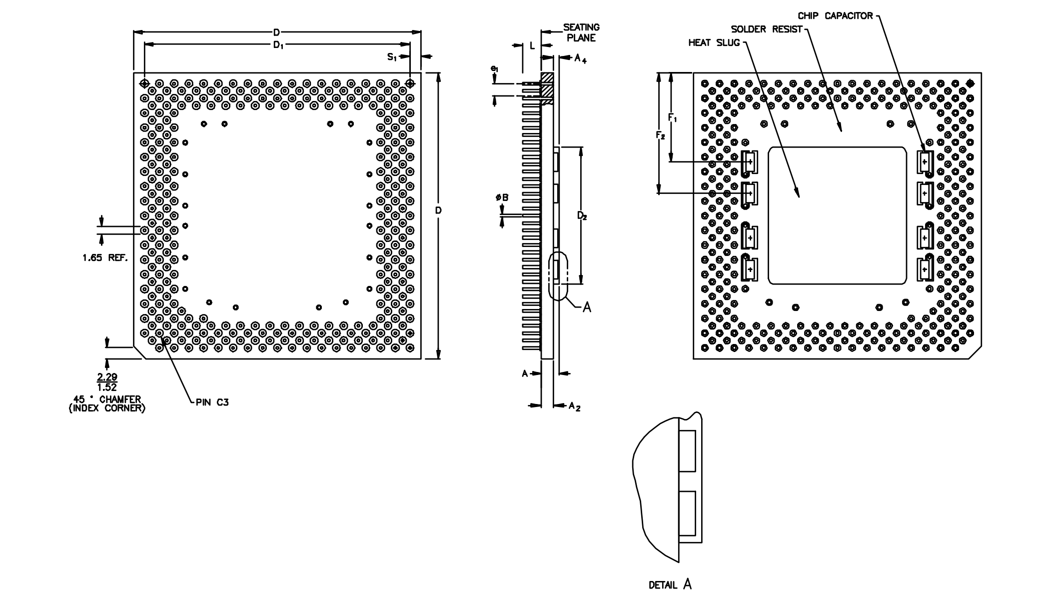


Figure 13. PPGA Package Dimensions

Table 19. PPGA Package Dimensions

Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
A	2.72	3.33		0.107	0.131	
A_1	1.83	2.23		0.072	0.088	
A_2	1.00			0.039		
B	0.40	0.51		0.016	0.020	
D	49.43	49.63		1.946	1.954	
D_1	45.59	45.85		1.795	1.805	
D_2	23.44	23.95		0.923	0.943	
e_1	2.29	2.79		0.090	0.110	
F_1	17.56			0.692		
F_2	23.04			0.907		
L	3.05	3.30		0.120	0.130	
N	296		Lead Count	296		Lead Count

Table 19. PPGA Package Dimensions

Symbol	Millimeters			Inches		
	Min	**Max**	**Notes**	**Min**	**Max**	**Notes**
S_1	1.52	2.54		0.060	0.100	

5.0. THERMAL SPECIFICATIONS

The Pentium processor with MMX technology is specified for proper operation when case temperature, T_{CASE}, (T_C) is within the specified range of 0°C to 70°C.

5.1. Measuring Thermal Values

To verify that the proper T_C is maintained, it should be measured at the center of the package top surface (opposite of the pins). The measurement is made in the same way with or without a heatsink attached. When a heatsink is attached, a hole (smaller than 0.150" diameter) should be drilled through the heatsink to allow probing the center of the package. See Figure 14 for an illustration of how to measure TC.

To minimize the measurement errors, it is recommended to use the following approach:

- Use 36-gauge or finer diameter K, T, or J type thermocouples. The laboratory testing was done using a thermocouple made by Omega* (part number 5TC-TTK-36-36).
- Attach the thermocouple bead or junction to the center of the package top surface using high thermal conductivity cements. The laboratory testing was done by using Omega Bond (part number OB-100).
- The thermocouple should be attached at a 90-degree angle as shown in Figure 14.
- The hole size should be smaller than 0.150' in diameter.
- Make sure there is no contact between thermocouple cement and heatsink base. The contact will affect the thermocouple reading.

5.1.1. THERMAL EQUATIONS AND DATA

For the Pentium processor with MMX technology, an ambient temperature, T_A (air temperature around the processor), is not specified directly. The only restriction is that T_C is met. To calculate T_A values, the following equations may be used:

$$T_A = T_C - (P * \Theta_{CA})$$

$$\Theta_{CA} = \Theta_{JA} - \Theta_{JC}$$

Where:

T_A and T_C = Ambient and case temperature. (°C)

Θ_{CA} = Case-to-ambient thermal resistance. (ºC/Watt)

Θ_{JA} = Junction-to-ambient thermal resistance. (ºC/Watt)

Θ_{JC} = Junction-to-case thermal resistance. (ºC/Watt)

P = Maximum power consumption (Watt)

Table 20 and Table 21 list the Θ_{JC} and Θ_{CA} values for the Pentium processor with MMX technology with passive heatsinks. Θ_{JC} is thermal resistance from die to package case. Θ_{JC} values shown in these tables are typical values. The actual Θ_{JC} values depend on actual thermal conductivity and process of die attach. Θ_{CA} is thermal resistance from package case to the ambient. Θ_{CA} values shown in these tables are typical values. The actual Θ_{CA} values depend on the heatsink design, interface between heatsink and package, the air flow in the system, and thermal interactions between processor and surrounding components through PCB and the ambient. Figure 15 and Figure 16 show Table 20 and Table 21 in graphical format.

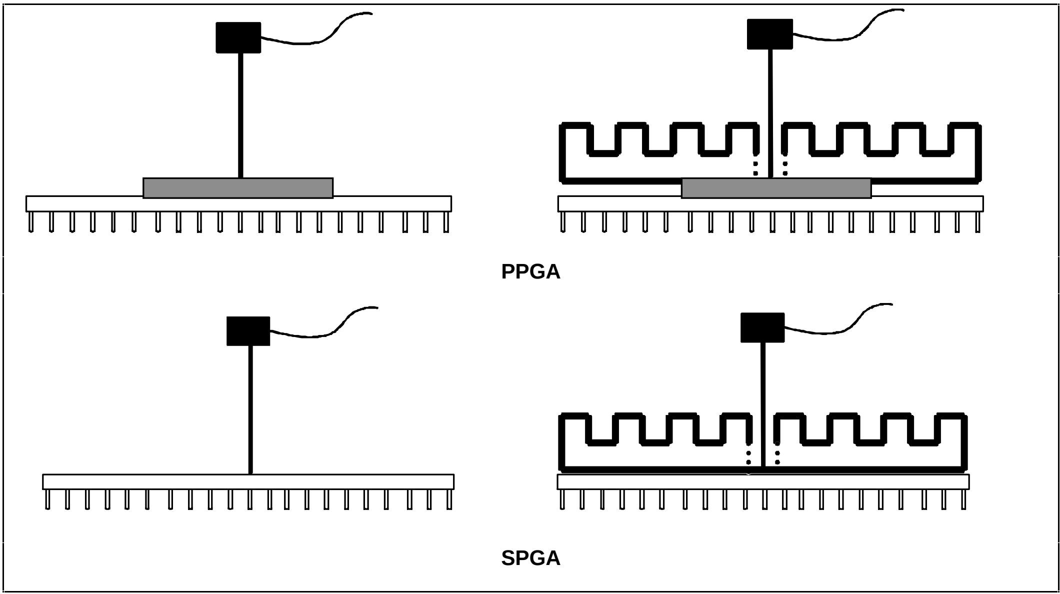


Figure 14. Technique fore Measuring T_C on PPGA and SPGA Packages

Table 20. Thermal Resistance for SPGA Packages

Heatsink Height (inches)	θ_{JC} (°C/Watt)	θ_{CA} (°C/Watt) vs. Laminar Airflow (linear ft/min)					
		0	100	200	400	600	800
0.25	0.9	9.2	8.1	6.7	4.6	3.7	3.1
0.35	0.9	8.9	7.6	6.1	4.1	3.4	2.9
0.45	0.9	8.5	7.1	5.4	3.7	3.0	2.6
0.55	0.9	8.2	6.6	4.8	3.3	2.7	2.4
0.65	0.9	7.8	6.1	4.4	3.1	2.5	2.2
0.80	0.9	7.1	5.4	4.0	2.9	2.3	2.1
1.00	0.9	6.4	4.8	3.7	2.7	2.2	1.9
1.20	0.9	6.0	4.4	3.4	2.5	2.1	1.9
1.40	0.9	5.5	4.0	3.1	2.3	2.0	1.8
Without Heatsink	1.4	14.4	13.4	12.1	9.7	8.0	7.0

NOTES:

Heatsinks are omni directional pin aluminum alloy.

Features were based on standard extrusion practices for a given height:

Pin size ranged from 50 to 129 mils

Pin spacing ranged from 93 to 175 mils

Based thickness ranged from 79 to 200 mils

Heatsink attach was 0.005" of thermal grease.

Attach thickness of 0.002" will improve performance approximately 0.3ºC/Watt.

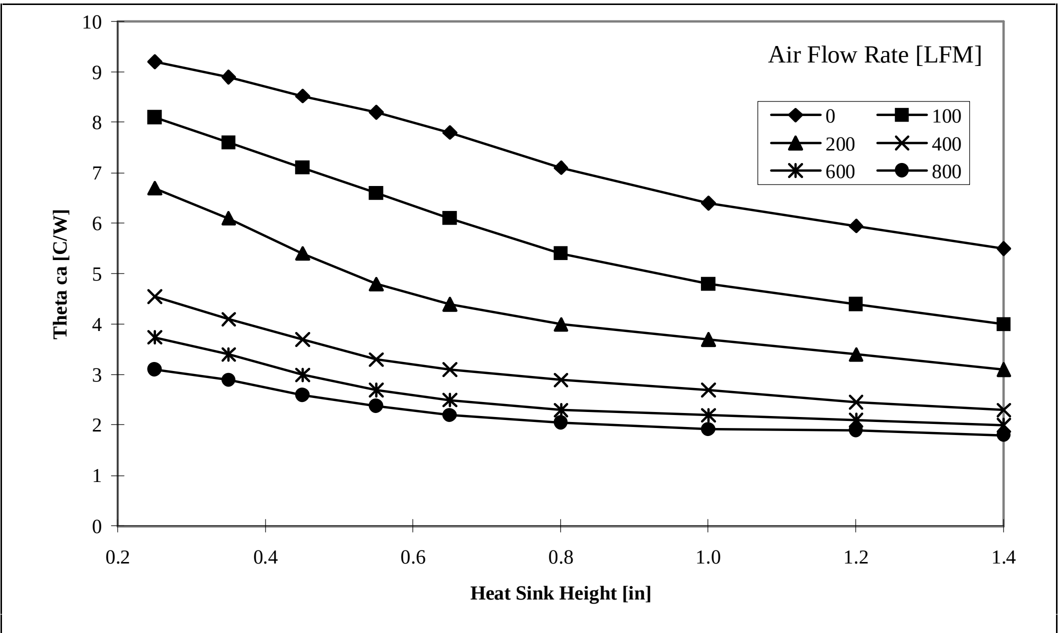


Figure 15. Thermal Resistance vs. Heatsink Height, SPGA Packages

Table 21. Thermal Resistances for PPGA Packages

Heat Sink Height (inches)	θ_{JC} (°C/Watt)	θ_{CA} (°C/Watt) vs. Laminar Airflow (linear ft/min)					
		0	100	200	400	600	800
0.25	0.4	8.9	7.8	6.4	4.3	3.4	2.8
0.35	0.4	8.6	7.3	5.8	3.8	3.1	2.6
0.45	0.4	8.2	6.8	5.1	3.4	2.7	2.3
0.55	0.4	7.9	6.3	4.5	3.0	2.4	2.1
0.65	0.4	7.5	5.8	4.1	2.8	2.2	1.9
0.80	0.4	6.8	5.1	3.7	2.6	2.0	1.8
1.00	0.4	6.1	4.5	3.4	2.4	1.9	1.6
1.20	0.4	5.7	4.1	3.1	2.2	1.8	1.6
1.40	0.4	5.2	3.7	2.8	2.0	1.7	1.5
None	1.2	12.9	12.2	11.2	7.7	6.3	5.4

NOTES:

Heatsinks are omni directional pin aluminum alloy.

Features were based on standard extrusion practices for a given height:

Pin size ranged from 50 to 129 mils

Pin spacing ranged from 93 to 175 mils

Based thickness ranged from 79 to 200 mils

Heatsink attach was 0.005" of thermal grease.

Attach thickness of 0.002" will improve performance approximately 0.3ºC/Watt.

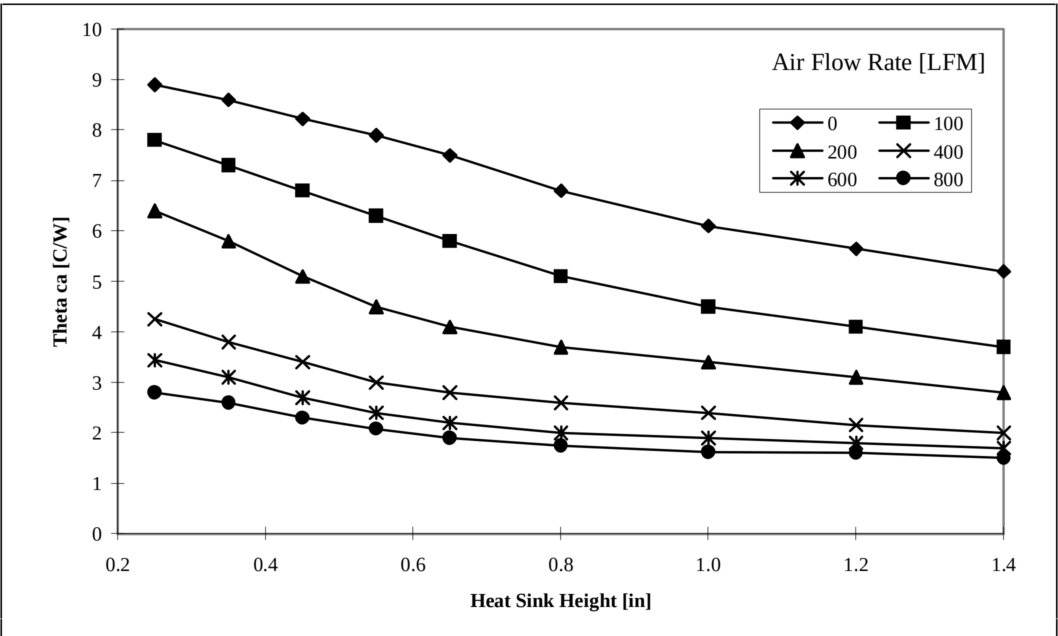


Figure 16. Thermal Resistance vs. Heatsink Height, PPGA Packages